

100V N-Channel Power SpeedFET

● Features

- AEC-Q101 Qualified
- Low $R_{DS(ON)}$ to minimize conductive loss
- Low Gate Charge for fast switching
- Low Thermal resistance

● Application

- SMPS 2nd Synchronous Rectifier
- Load switch
- BLDC Motor driver

● General Description

It combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$.

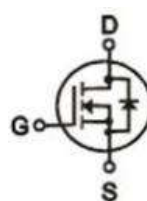
● Ordering Information:

Part NO.	KPRA250N10N-V
Marking	ZMS250N10
Packing Information	REEL TAPE
Basic ordering unit (pcs)	3000

● Absolute Maximum Ratings ($T_C = 25^\circ\text{C}$)

Parameter	Symbol	Conditions	Rating	Unit
Drain-Source Voltage	V_{DS}	$25^\circ\text{C} \leq T_J \leq 175^\circ\text{C}$	100	V
Gate-Source Voltage	V_{GS}	Pulsed ^①	+20/-20	V
	V_{GS}	DC; $T_J \leq 175^\circ\text{C}$	+15/-5	V
Continuous Drain Current	I_D	$T_C = 25^\circ\text{C}$	31	A
	I_D	$T_C = 75^\circ\text{C}$	23	A
	I_D	$T_C = 100^\circ\text{C}$	19	A
Pulsed Drain Current	I_{DM}	pulsed; $t_p \leq 10 \mu\text{s}$; $T_{mb} = 25^\circ\text{C}$;	93	A
Total Power Dissipation	P_D	$T_C = 25^\circ\text{C}$	65	W
Total Power Dissipation	P_D	$T_A = 25^\circ\text{C}$	3.0	W
Operating Junction Temperature	T_J		-55 to 175	$^\circ\text{C}$
Storage Temperature	T_{STG}		-55 to 175	$^\circ\text{C}$
Single Pulse Avalanche Energy	E_{AS}	$L = 0.1\text{mH}$, $V_{GS} = 10\text{V}$, $R_g = 25\Omega$, $T_J = 25^\circ\text{C}$	18	mJ
ESD Level (HBM)			CLASS 1C	

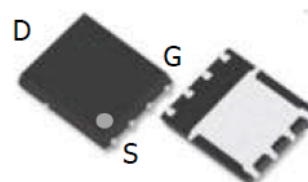
● Product Summary



$$V_{DS} = 100\text{V}$$

$$R_{DS(ON)} = 25\text{m}\Omega$$

$$I_D = 31\text{A}$$



DFN5 x 6

● Thermal resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case	R_{thJC}	-	-	1.7	°C/W
Thermal resistance, junction - ambient ^②	R_{thJA}	-	-	50	°C/W
Soldering temperature, wavesoldering for 10s	T_{sold}	-	-	260	°C

● Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	100			V
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\mu A$	1.3		2.5	V
Drain-Source Leakage Current	I_{DSS}	$V_{DS} = 100V, V_{GS} = 0V$			1.0	μA
Gate- Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20V, V_{DS} = 0V$			± 100	nA
Static Drain-source On Resistance	$R_{DS(ON)}$	$V_{GS} = 10V, I_D = 9A$		25	32	m Ω
	$R_{DS(ON)}$	$V_{GS} = 4.5V, I_D = 6A^{\textcircled{3}}$		32	41	m Ω
Forward Transconductance	g_{FS}	$V_{DS} = 10V, I_D = 4A$		5		S

● Electronic Characteristics

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Gate Resistance	R_g	$f = 1MHz$		0.4		Ω
Input capacitance	C_{iss}	$f = 1MHz$ $V_{DS} = 25V$	-	550	-	pF
Output capacitance	C_{oss}		-	292	-	
Reverse transfer capacitance	C_{rss}		-	7.4	-	

● Gate Charge characteristics($T_a = 25^\circ C$)

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Total gate charge	Q_g	$V_{DD} = 25V$ $I_D = 8A$ $V_{GS} = 10V$	-	13	-	nC
	$Q_g(4.5v)$			6.0		
Gate - Source charge	Q_{gs}		-	2.0	-	
Gate - Drain charge	Q_{gd}		-	3.2	-	

Fig.1 Gate-Charge Characteristics

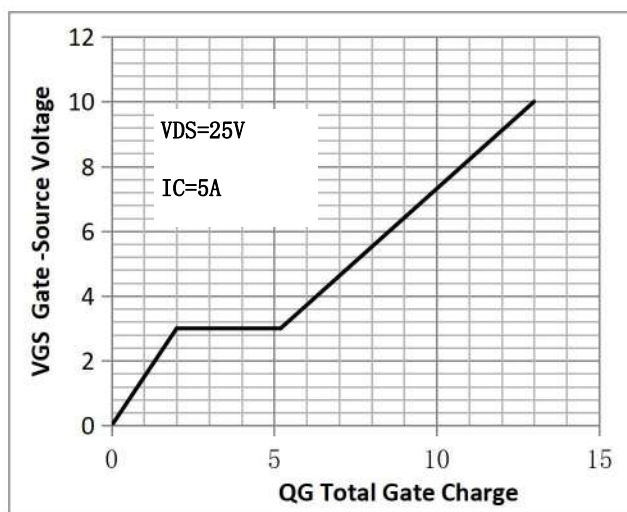


Fig.2 Capacitance Characteristics

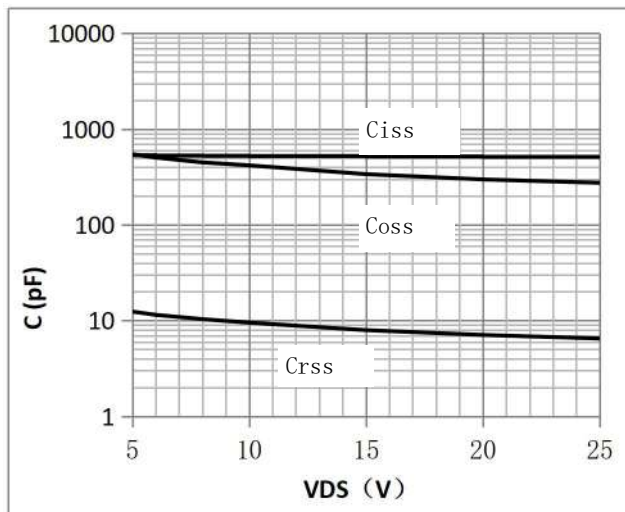


Fig.3 Power Dissipation

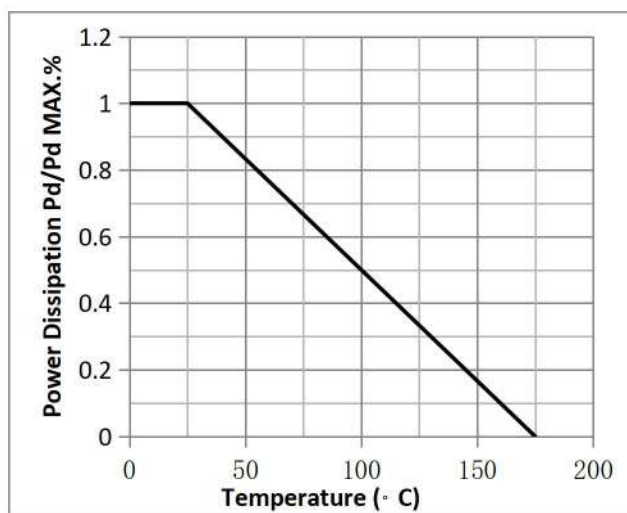


Fig.4 Typical output Characteristics

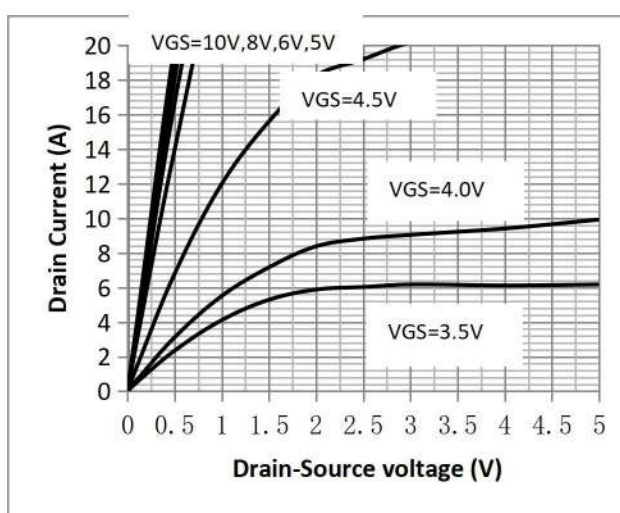


Fig.5 Threshold Voltage V.S Junction Temperature

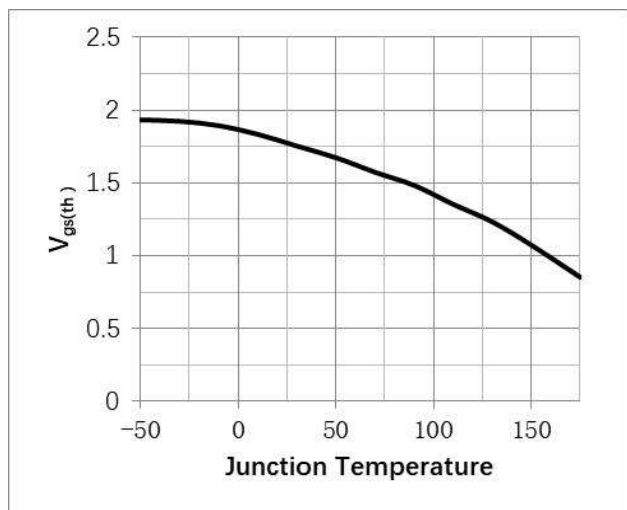


Fig.6 Resistance V.S Drain Current

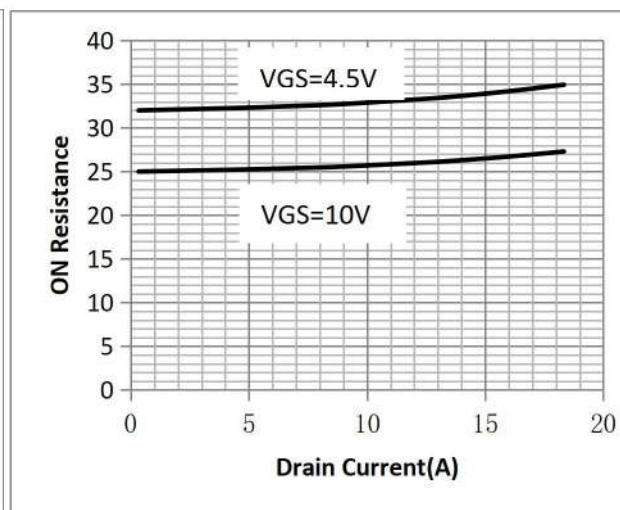


Fig.7 On-Resistance VS Gate Source Voltage

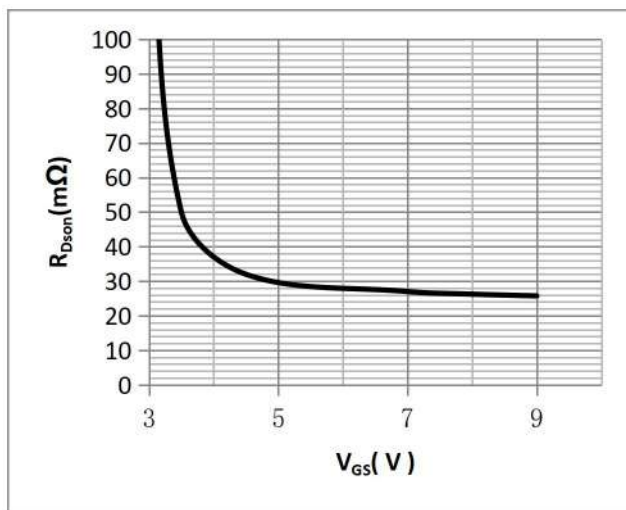


Fig.8 On-Resistance V.S Junction Temperature

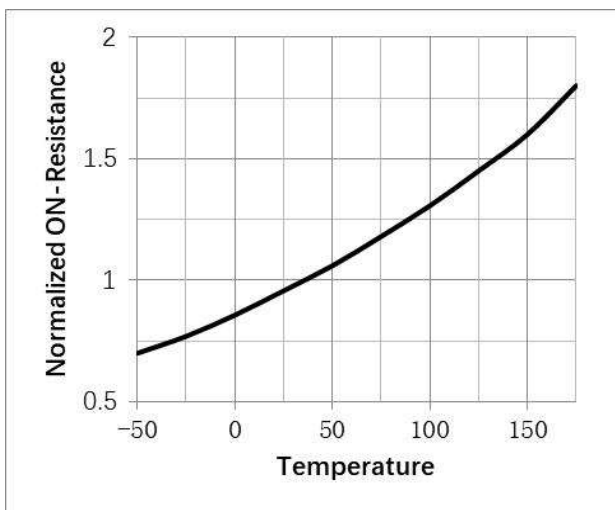


Fig.9 SOA Maximum Safe Operating Area

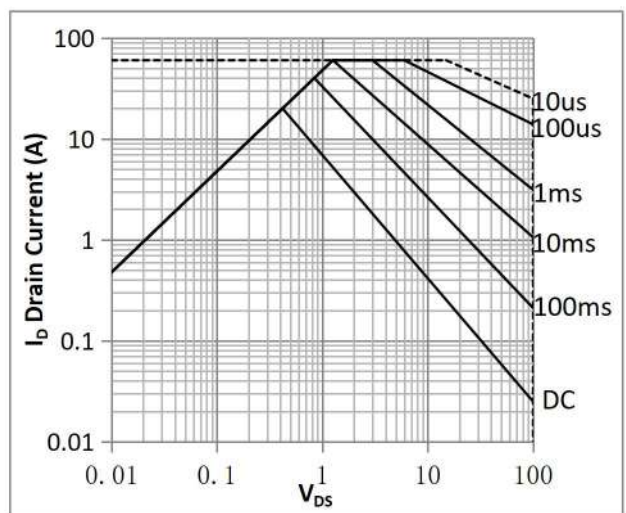


Fig.10 ID-Junction Temperature

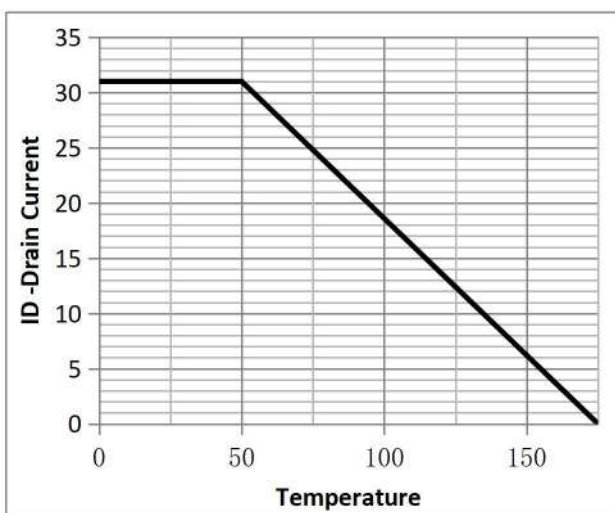


Fig.11 Switching Time Measurement Circuit

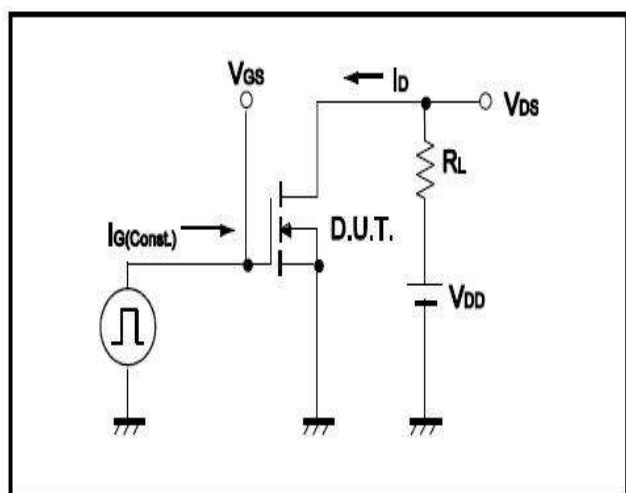


Fig.12 Gate Charge Waveform

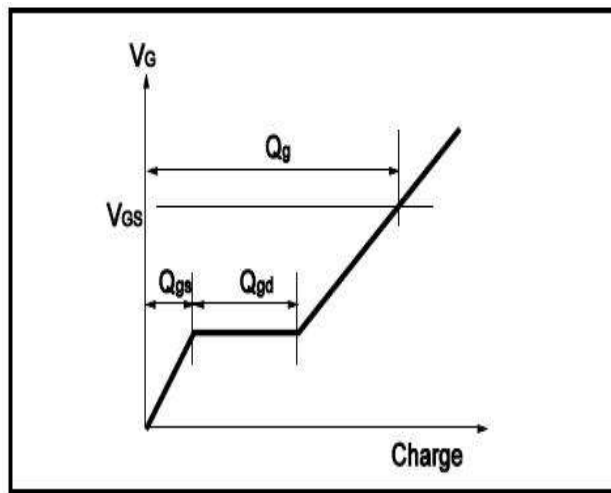


Fig.13 Switching Time Measurement Circuit

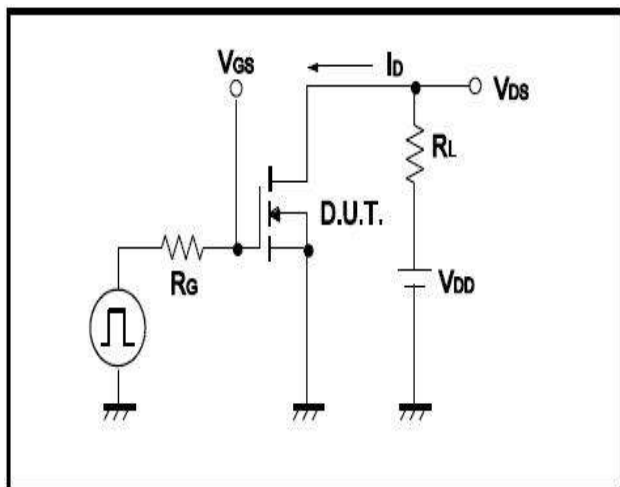
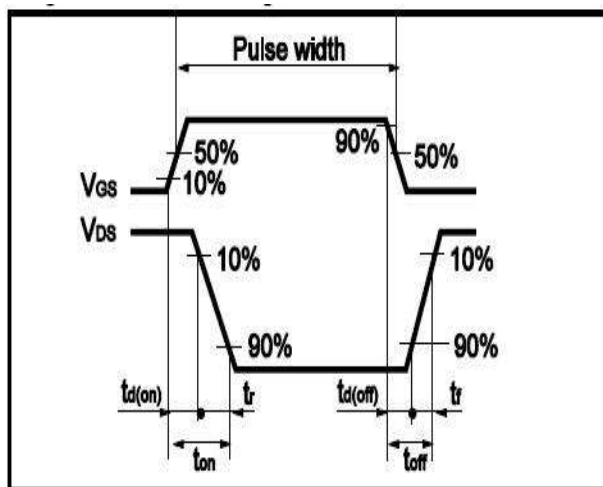
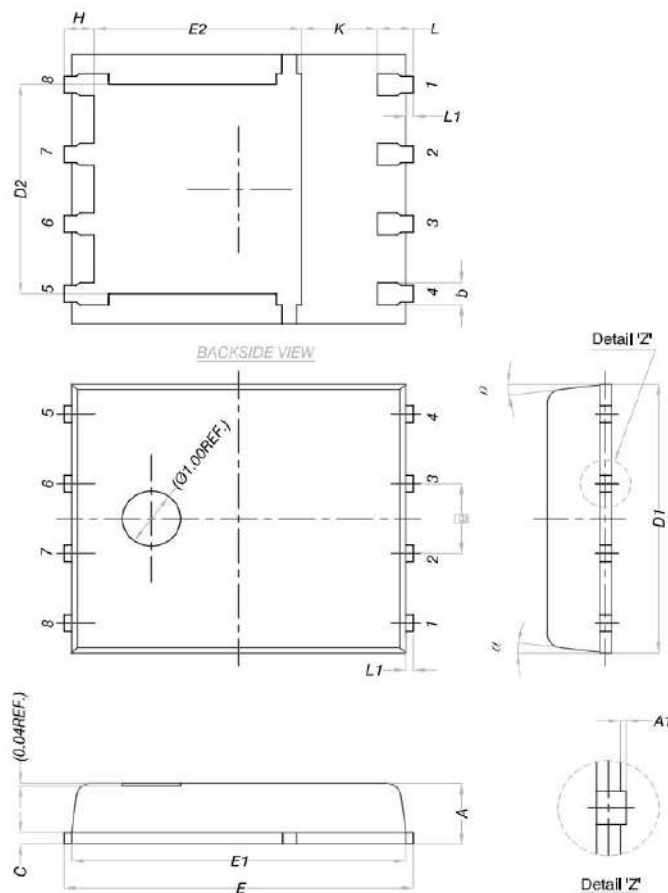


Fig.14 Gate Charge Waveform



• **Dimensions (DFN5×6)**

Unit: mm



DIM.	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0	-	0.05
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e	1.27 BSC		
H	0.41	0.51	0.61
K	1.10	-	-
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
α	0°	-	12°

Note: ① Pulse Test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$;

② Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate;

③ $V_{gs} \geq 4.5\text{V}$ is required for practical application.