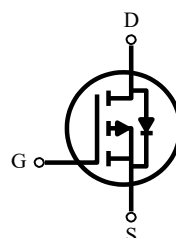


P-Channel High Density Trench MOSFET

FEATURES

- Super high dense cell trench design for low $R_{DS(on)}$.
- Rugged and reliable.
- Surface Mount package.

SOT-323



PRODUCT SUMMARY

V_{DSS}	I_D	$R_{DS(on)}$ (m-ohm) Max
-20V	-2.5	120 @ $V_{GS} = 4.5V$
	-2	180 @ $V_{GS} = 2.5V$

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-20	V
Gate-Source Voltage	V_{GS}	± 12	V
Drain Current-Continuous ^a @ $T_A = 25^\circ C$ -Pulse ^b	I_D	-2.5	A
	I_{DM}	-8	A
Drain-Source Diode Forward Current ^a	I_S	-0.75	A
Maximum Power Dissipation ^a	P_D	1.25	W
		0.75	
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to 150	$^\circ C$

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient ^a	R_{thJA}	100	$^\circ C/W$
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Note

a. Surface Mounted on FR4 Board, $t \leq 10sec$.

b. Pulse width limited by maximum junction temperature.

ELECTRICAL CHARACTERISTICS (T_A = 25 °C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V , I _D = -250uA	-20			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -20V , V _{GS} = 0V			-1	uA
Gate-Body Leakage	I _{GSS}	V _{GS} = ±12V , V _{DS} = 0V			-100	nA
ON CHARACTERISTICS ^b						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250uA	-0.45	-0.65	-0.95	V
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = -4.5V , I _D = -2.5A		110	120	m-ohm
		V _{GS} = -2.5V , I _D = -2.0A		160	180	m-ohm
DRAIN-SOURCE DIODE CHARACTERISTICS ^b						
Diode Forward Voltage	V _{SD}	V _{GS} = 0V , I _S = -0.75A			-1.2	V
DYNAMIC CHARACTERISTICS ^c						
Input Capacitance	C _{ISS}	V _{DS} = -6V , V _{GS} = 0V f = 1.0MHz		664		pF
Output Capacitance	C _{OSS}			154		pF
Reverse Transfer Capacitance	C _{RSS}			129		pF
SWITCHING CHARACTERISTICS ^c						
Turn-On Delay Time	t _{D(ON)}	V _{DD} = -6V , I _D = -1A V _{GEN} = -4.5V R _L = 6 ohm R _{GEN} = 6 ohm		8.6		ns
Rise Time	t _r			3.0		ns
Turn-Off Delay Time	t _{D(OFF)}			39.2		ns
Fall Time	t _f			11.2		ns
Total Gate Charge	Q _g	V _{DS} = -6V I _D = -2.8A V _{GS} = -4.5V		6.72		nC
Gate-Source Charge	Q _{gs}			1.12		nC
Gate-Drain Charge	Q _{gd}			1.04		nC

Note

b. Pulse Test Pulse width ≤ 300us , Duty Cycle ≤ 2% .

c. Guaranteed by design , not subject to production testing .

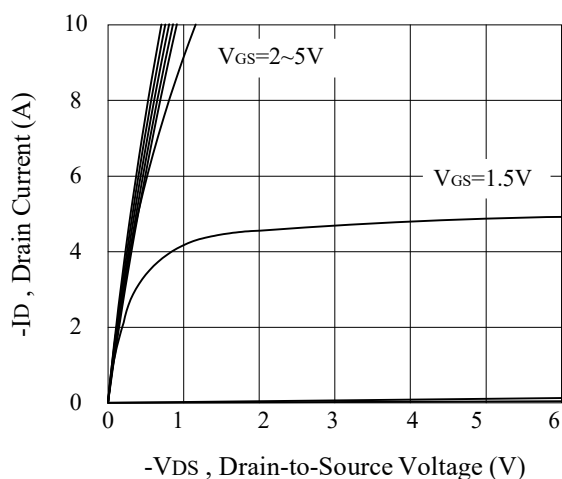


Figure 1. Output Characteristics

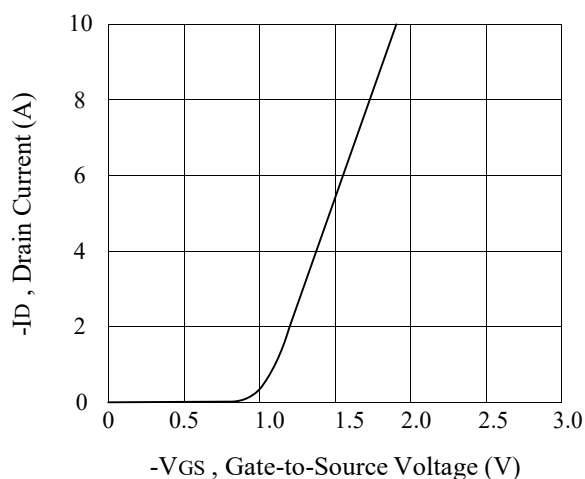


Figure 2. Transfer Characteristics

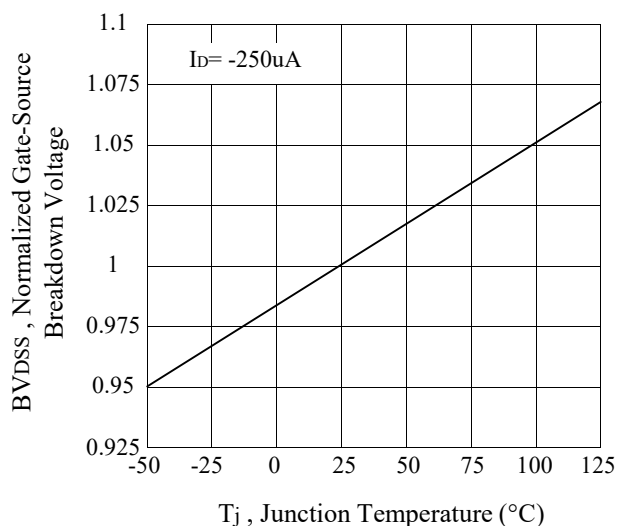


Figure 3. Breakdown Voltage Variation with Temperature

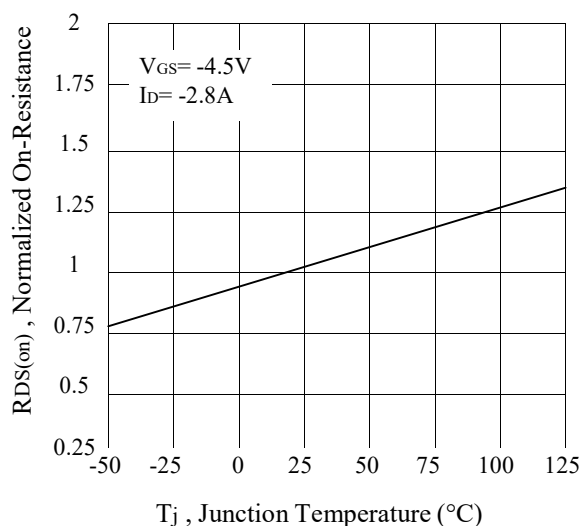


Figure 4. On-Resistance Variation with Temperature

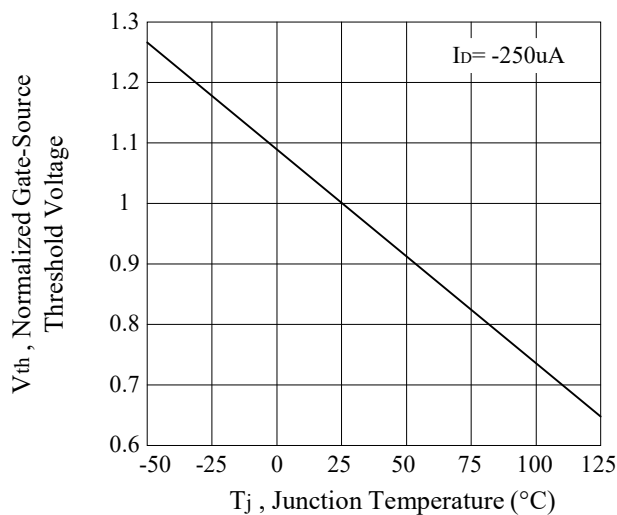


Figure 5. Gate Threshold Variation with Temperature

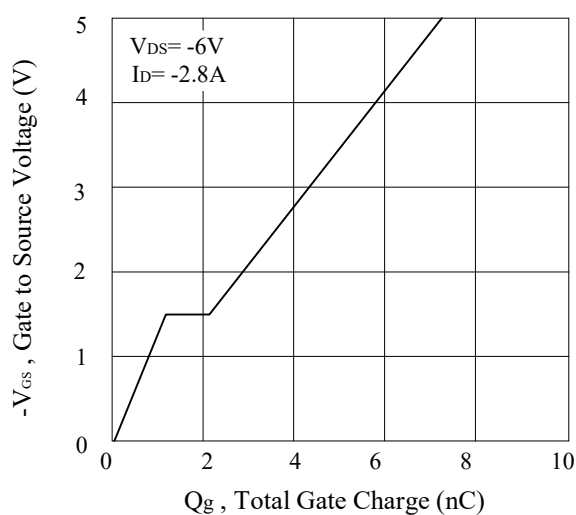
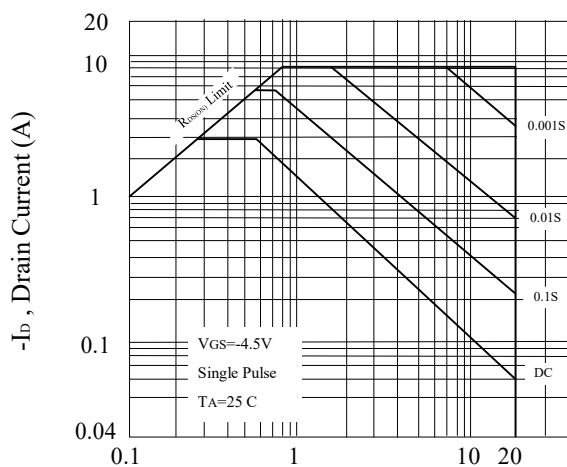
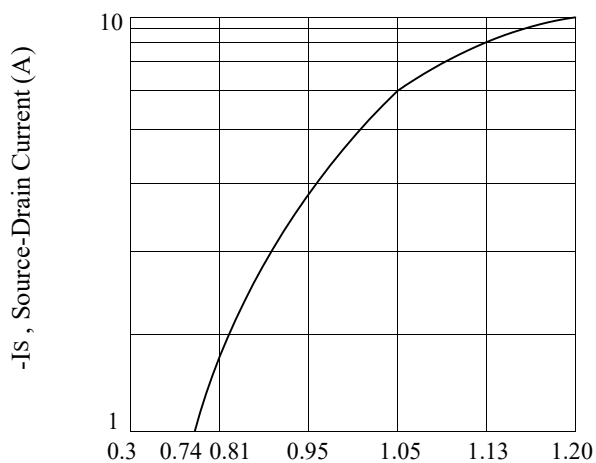


Figure 6. Gate Charge



-VDS, Drain-Source Voltage (V)
 Figure 7. Maximum Safe Operating Area



-VSD, Body Diode Forward Voltage (V)
 Figure 8. Body Diode Forward Voltage Variation with Source Current

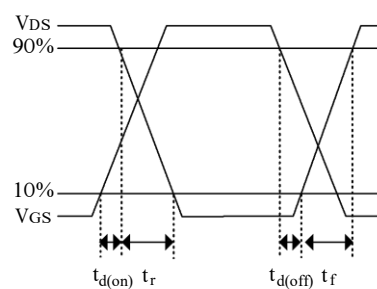
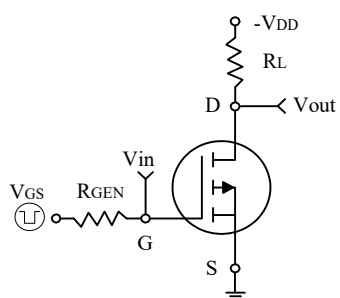


Figure 9. Switching Test Circuit and Switching Waveforms

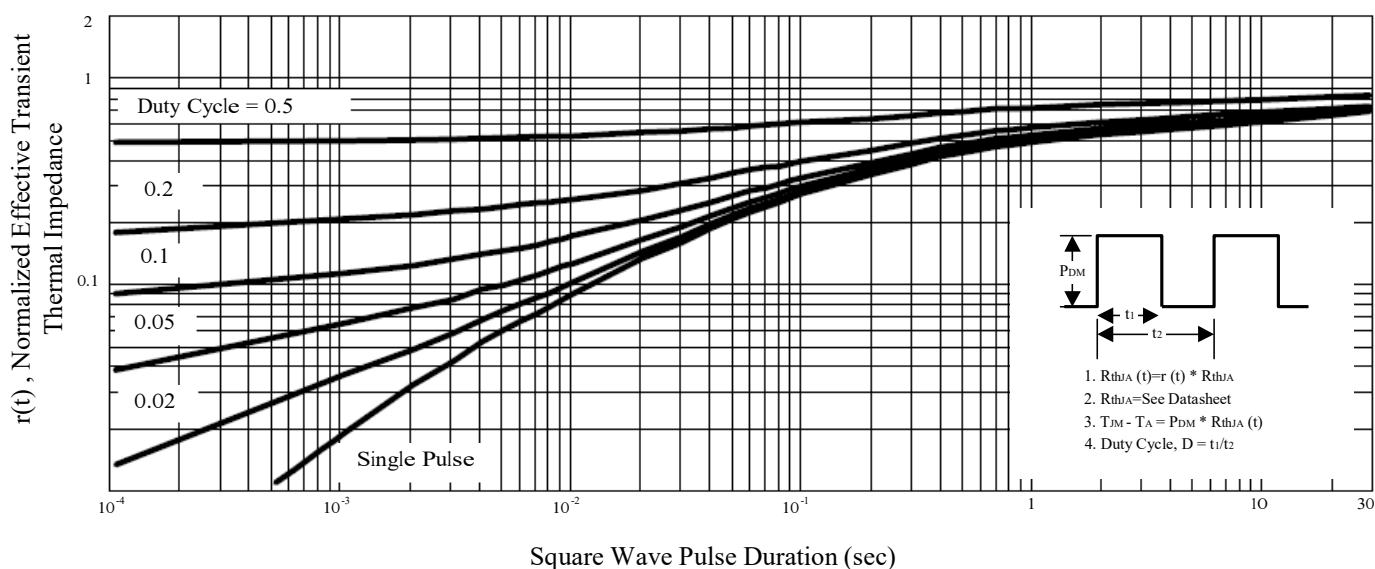


Figure 10. Normalized Thermal Transient Impedance Curve