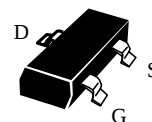


N-Channel High Density Trench MOSFET

FEATURES

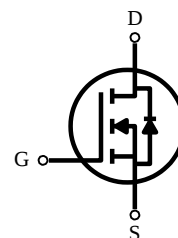
- Super high dense cell trench design for low $R_{DS(on)}$.
- Rugged and reliable.
- Surface Mount package.

SOT-23



PRODUCT SUMMARY

V_{DSS}	I_D	$R_{DS(on)}$ (m Ω) Max
40V	3.8A	38 @ $V_{GS} = 10V$
	2.7A	52 @ $V_{GS} = 4.5V$



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous ^a @ $T_A = 25^\circ\text{C}$ -Pulse ^b	I_D	3.8	A
	I_{DM}	15	A
Drain-Source Diode Forward Current ^a	I_S	2.5	A
Maximum Power Dissipation ^a	P_D	$T_A=25^\circ\text{C}$ 1.25	W
		$T_A=75^\circ\text{C}$ 0.75	
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to 150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient ^a	R_{thJA}	100	$^\circ\text{C/W}$
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Note :

a. Surface Mounted on FR4 Board , $t \leq 10\text{sec}$.

b. Pulse width limited by maximum junction temperature.

ELECTRICAL CHARACTERISTICS ($T_A = 25\text{ }^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ ^c	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V , I _D = 250uA	40			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 24V , V _{GS} = 0V			1	uA
Gate-Body Leakage	I _{GSS}	V _{GS} = ±12V , V _{DS} = 0V			±100	nA
ON CHARACTERISTICS ^b						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250uA	1	1.5	2.5	V
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10V , I _D = 4.6A		30	38	mΩ
		V _{GS} = 4.5V , I _D = 3.8A		42	52	
Forward Transconductance	g _{fs}	V _{DS} = 5V , I _D = 5A		8		S
DRAIN-SOURCE DIODE CHARACTERISTICS ^b						
Diode Forward Voltage	V _{SD}	V _{GS} = 0V , I _s = 1.0A			1.2	V
DYNAMIC CHARACTERISTICS ^c						
Input Capacitance	C _{ISS}	V _{DS} = 15V , V _{GS} = 0V f = 1.0MHz		452		pF
Output Capacitance	C _{OSS}			51		pF
Reverse Transfer Capacitance	C _{RSS}			38		pF
SWITCHING CHARACTERISTICS ^c						
Turn-On Delay Time	t _{D(ON)}	V _{DD} = 15V , I _D = 1A V _{GEN} = 10V R _L = 15 Ω R _{GEN} = 6 Ω		7.8		ns
Rise Time	t _r			2.1		ns
Turn-Off Delay Time	t _{D(OFF)}			29		ns
Fall Time	t _f			2.1		ns
Total Gate Charge	Q _g	V _{DS} = 15V I _D = 3A V _{GS} = 10V		5		nC
Gate-Source Charge	Q _{gs}			1.54		nC
Gate-Drain Charge	Q _{gd}			1.84		nC

Note :

b. Pulse Test : Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.

c. Guaranteed by design, not subject to production testing.

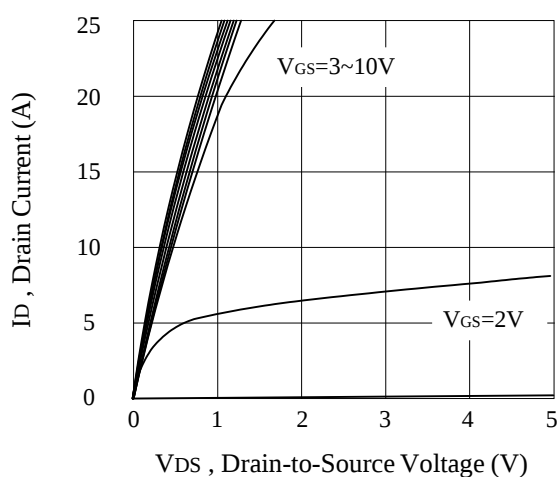


Figure 1. Output Characteristics

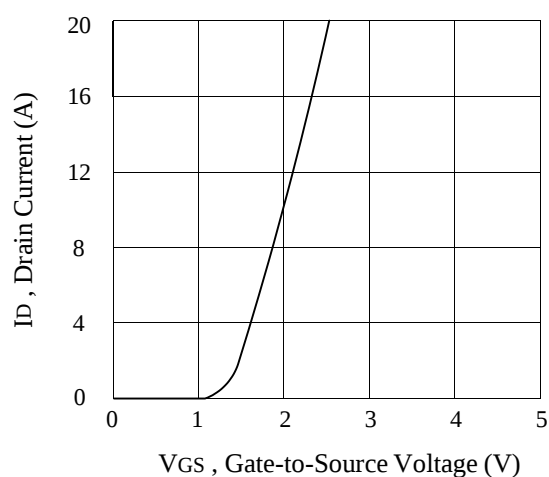


Figure 2. Transfer Characteristics

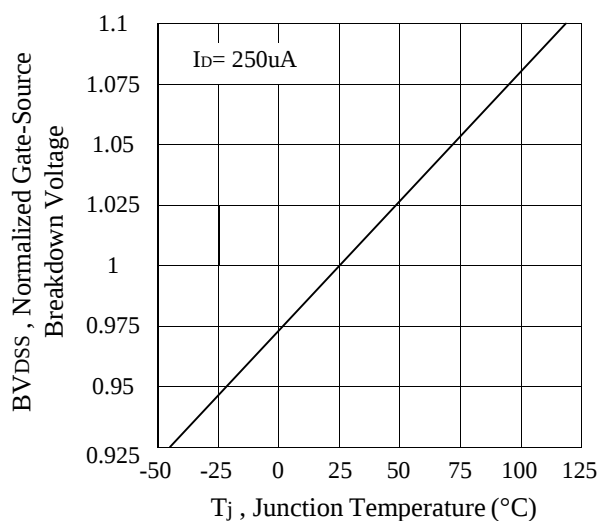


Figure 3. Breakdown Voltage Variation with Temperature

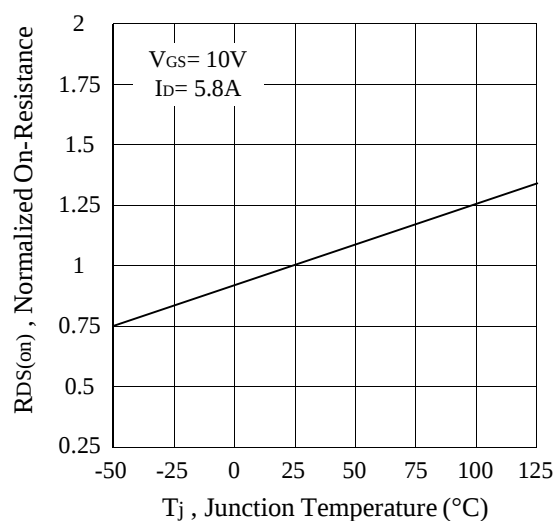


Figure 4. On-Resistance Variation with Temperature

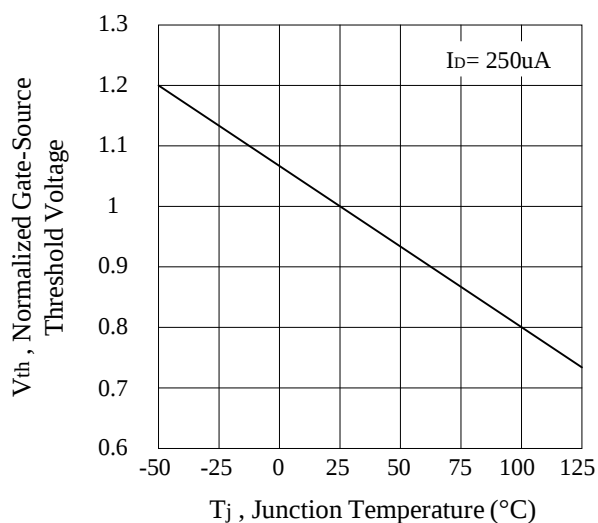


Figure 5. Gate Threshold Variation with Temperature

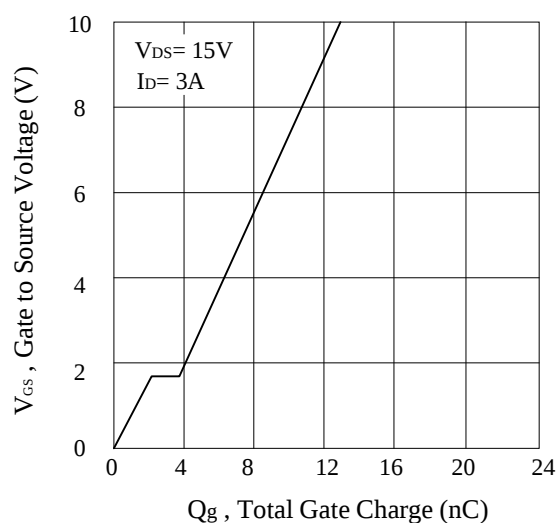
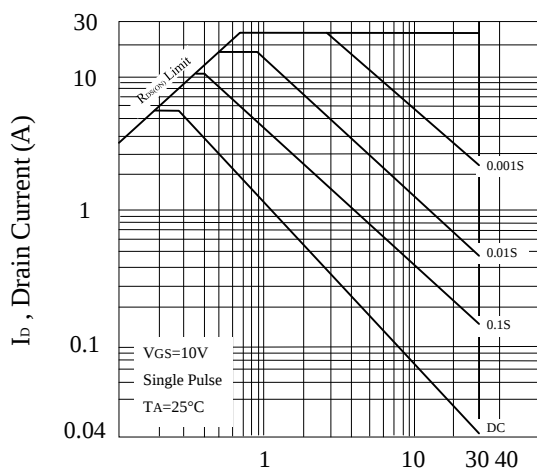
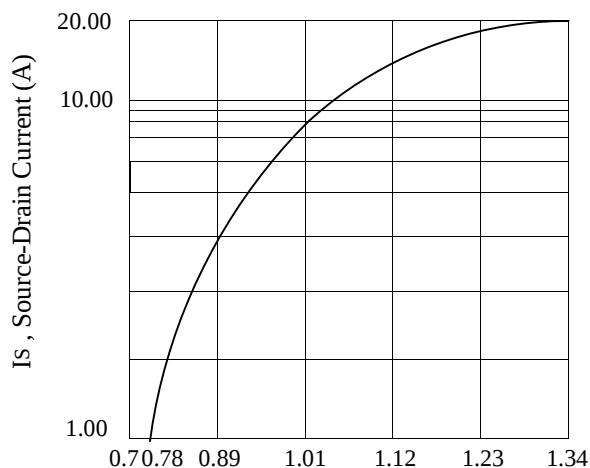


Figure 6. Gate Charge



VDS, Drain-Source Voltage (V)

Figure 7. Maximum Safe Operating Area



VSD, Body Diode Forward Voltage (V)

Figure 8. Body Diode Forward Voltage Variation with Source Current

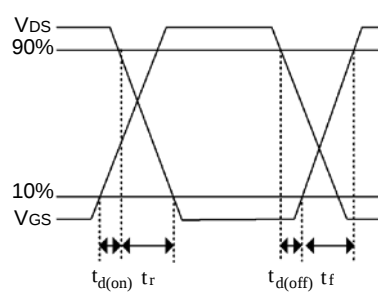
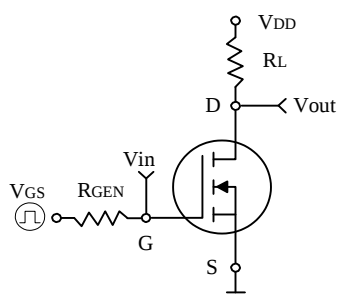


Figure 9. Switching Test Circuit and Switching Waveforms

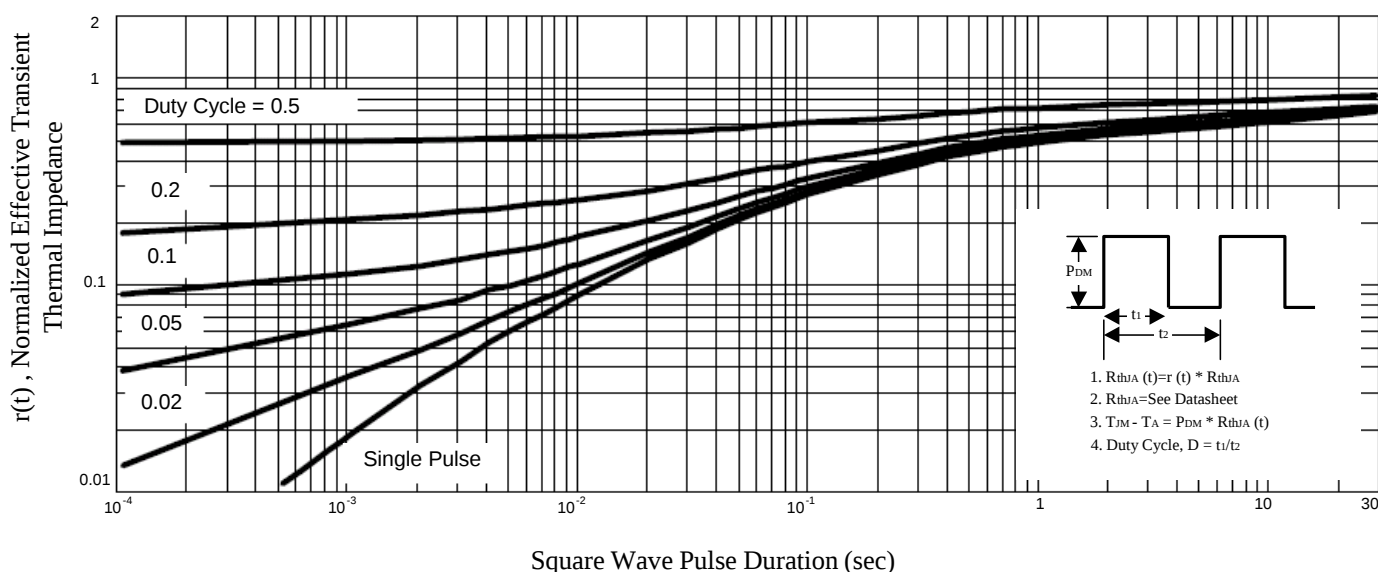


Figure 10. Normalized Thermal Transient Impedance Curve