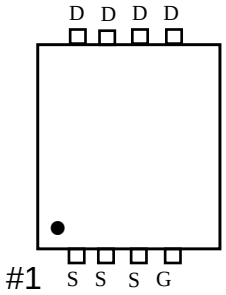
N-Channel MOSFET

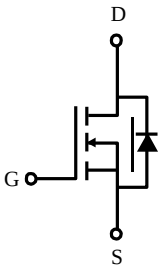
FEATURES

- Super high dense cell trench design for low $R_{DS(on)}$.
- Rugged and reliable.
- Surface Mount package.

PDFN5x6



PRODUCT SUMMARY		
$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
150V	16.4mΩ	50A



PARAME TERS TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gata-Source voltage		V_{GS}	±20	V
Continuous Drain current	T_C = 25℃	I_D	50	A
	T_C = 100 ℃		36	
Puised Drain Current[a]		I_{DM}	190	
Avalanche Current	L=0.1mH	I_{AS}	22	
Avalanche Energy		E_{AS}	272	mJ
Power Dissipation	T_C = 25 ℃	P_D	100	W
	T_C = 100 ℃		40	
Operaing junction & Storege Temperature Range		T_s,T_{stg}	-55 to 150	℃

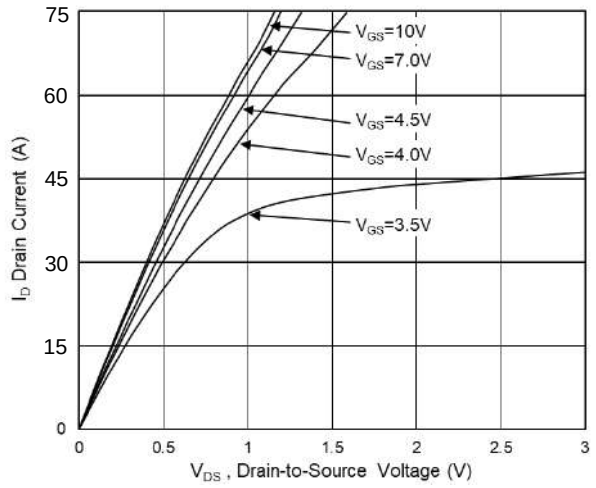
THERMAL CHARACTERISTICS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	$R_{\theta Jc}$ [d]		1.25	℃/W
Junction-to-Ambient	$R_{\theta JA}$		52	℃/W

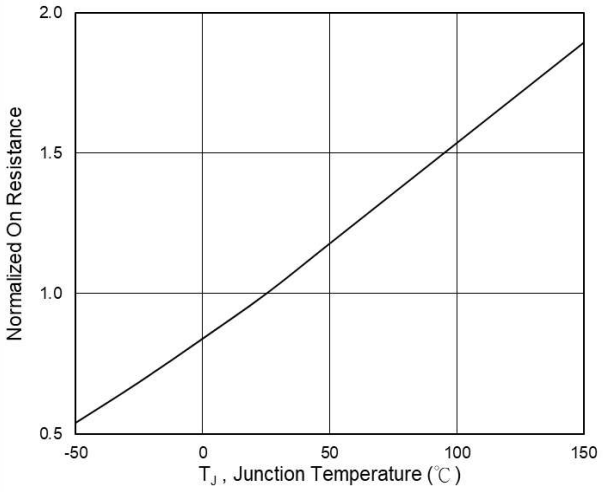
PARAMETER	SYNBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltege	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250μA	150			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	2	3	4	V
Gate-Body Leakage	I_{GSS}	V_{DS}=0V,V_{GS}=± 20V			±100	nA
Zero Gate Voltage Dain Current	I_{DSS}	V_{DS}=120V,V_{GS}=0 V			1	μA
		V_{DS}=120V,V_{GS}=0V,T_J=125 ℃			30	μA
Drain-Source On- State Resistance[b]	$R_{DS(ON)}$	V_{GS}=10V,I_D=20A		16.4	20	mΩ
Forward Trans conductance[b]	g_{fs}	V_{DS}=5V,I_D=20A		50		S
DYNAMIC[c]						
Input Capacitance	C_{iss}	V_{GS}=0V,V_{DS}=75V,f=1MHz		1832		pF
Output Capacitance	C_{oss}			148		pF
Reverse Transfer Capacitance	C_{rss}			8.2		pF
Gate Resistance	R_G	V_{GS}=0V,f=1MHz		2.3		Ω
Total Gate Charge[2]	$Q_{g(vgs=10V)}$	V_{DS}=75V$_{(BR)DSS}$, I_D = 20A		22		nC
Gate Source Charge[2]	$Q_{gS(VGS=10V)}$			7.5		nC
Gate-Drain Charge[2]	$Q_{gd(VGS=10V)}$			4.2		nC
Tum-On Delay Time[2]	$t_{d(on)}$	V_{DS}=175V, I_D=10A,V_{GS}=10V.R_{GS}=3.3Ω		11.3		nS
Rise Time[2]	t_r			5.2		nS
Tum-Off Delay Time[2]	$t_{d(off)}$			21.2		nS
Fall Time[2]	t_r			4.5		nS
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS(T_J=25℃)						
Continuous Current	I_S				50	A
Forward Voltage[1]	V_{SD}	I_F=I_S,V_{GS}=0V			1.2	V
Reverse Recovery Time	T_{rr}	I_F=20V,d_{1f}/d_t=100A/μs		70		nS
Reverse Recovery Charge	Q_{rr}	I_F=20V,d_{1f}/d_t=100A/μs		154.7		nC

Note

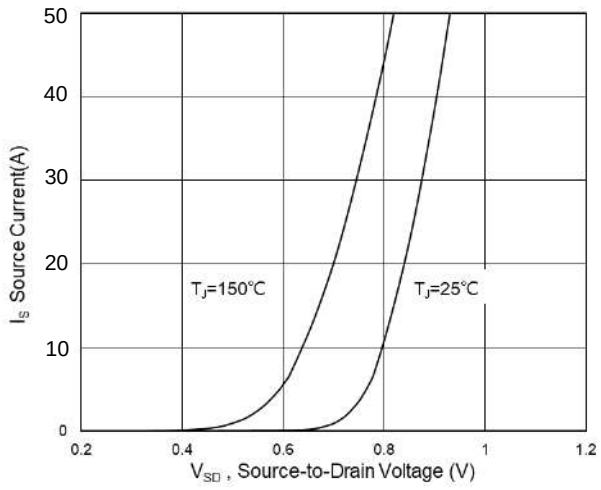
a. This current is chip limited, whiich is calculated based on Rthjc.
b. Pulse Test Pulse width ≤ 300usec , Duty Cycle ≤ 2% .
c. Independent of operating production testing .
d. Device mounted on FR-4 substrate PC board with 2oz copper in 1inch square cooling area.



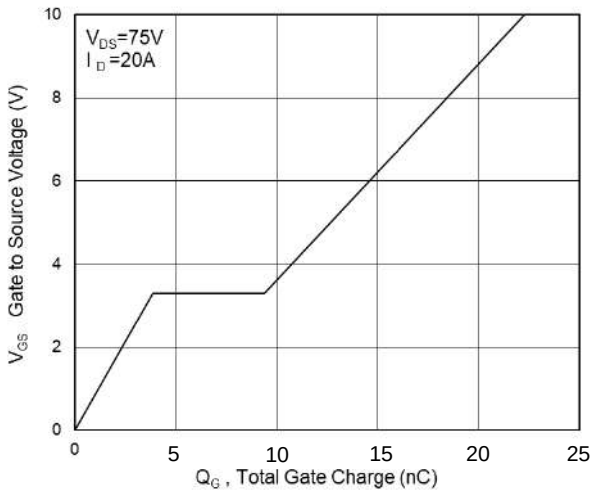
Typical Output Characteristics



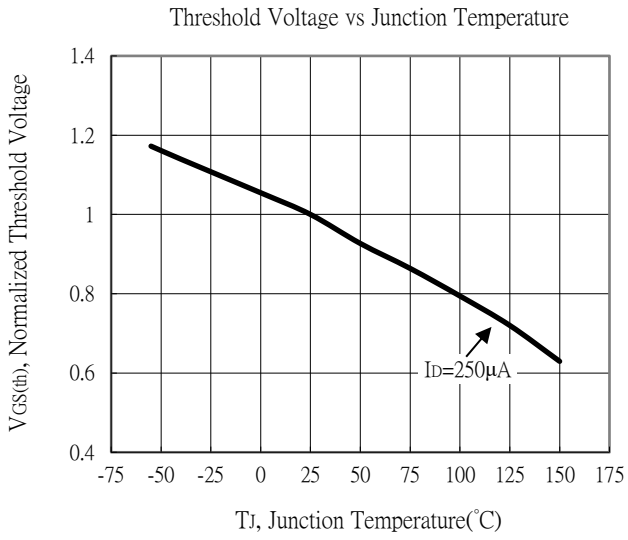
Normalized R_{DSON} vs T_J

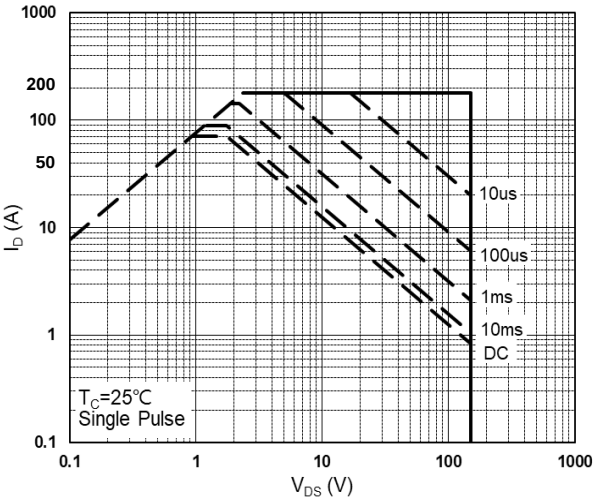


Source Drain Forward Characteristics

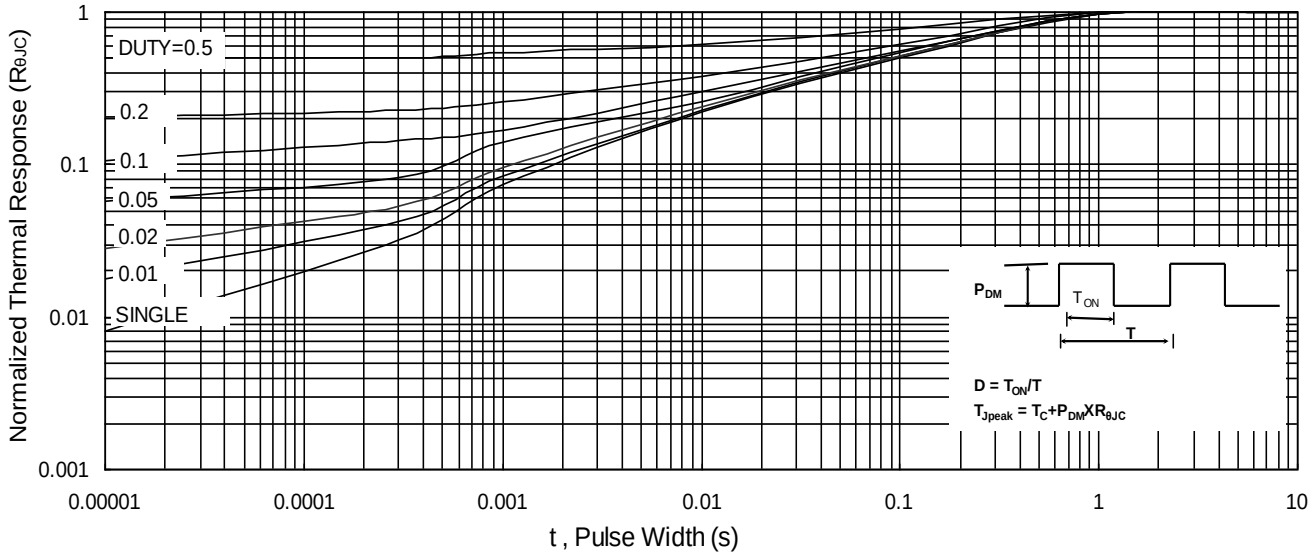


Gate-Charge Characteristics

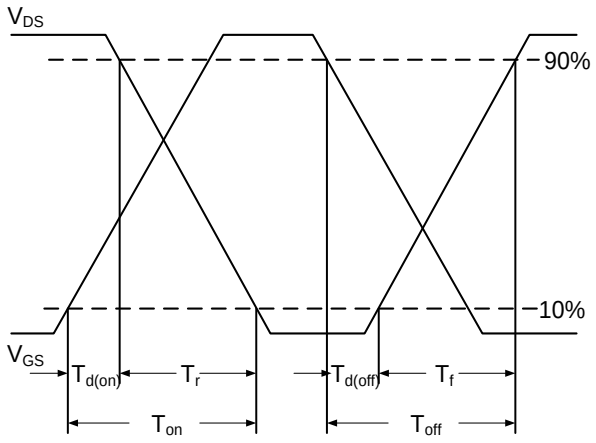




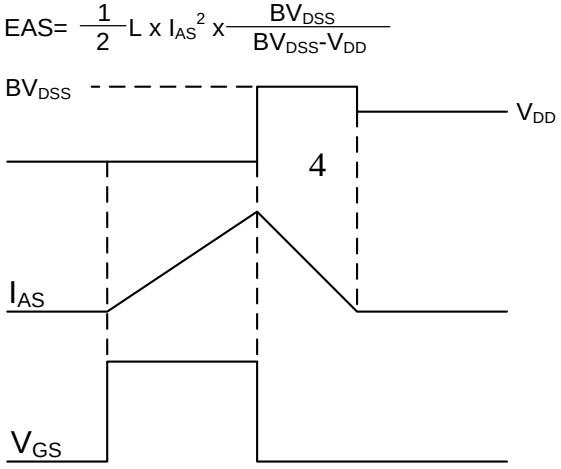
Safe Operating Area



Normalized Maximum Transient Thermal Impedance



Switching Time Waveform



Unclamped Inductive Waveform