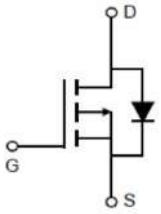
-60V P-Channel Enhancement Mode MOSFET

General Description

The BSS84 uses SGT technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications. The package form is SOT-23, which accords with the ROHS standard and Halogen Free standard.

Inner Equivalent Principium Chart



Features

- V_{DS} = -60 V I_D = -0.3A
- $R_{DS(ON)}$ < 2.5Ω @ V_{GS}= -10V
- Fast Switching
- Low Gate Charge and $R_{DS(ON)}$
- Low Reverse transfer capacitances

Marking and Pin Assignment

Applications

- DC-DC Converter
- Portable Equipment
- Power Management

Package Marking and Ordering Information

Marking	Part Number	Package	Packing	Qty.
6T10A	BSS84	SOT-23	Reel	3000 Pcs

Absolute Maximum Ratings

Symbol	Parameter		Value	Units
V_{DSS}	Drain-to-Source Voltage		-60	V
I_D	Continuous Drain Current	T_C=25℃	-0.30	A
	Continuous Drain Current	T_C=100℃	-0.19	A
I_{DM}[a1]	Pulsed Drain Current		-1.20	A
V_{GS}	Gate-to-Source Voltage		±20	V
P_D	Power Dissipation		0.35	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range		150, -55 to 150	℃
T_L	Maximum Temperature for Soldering		260	℃

Thermal Characteristics

Symbol	Parameter	Value	Units
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	357	℃/W

Electrical Characteristic (T_A = 25 °C, unless otherwise specified)

Static Characteristics						
Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	V_{GS}=0V, I_D=-250μA	-60	--	--	V
I_{DSS}	Drain to Source Leakage Current	V_{DS}=-60V, V_{GS}=0V	--	--	1.0	μA
$I_{GSS(F)}$	Gate to Source Forward Leakage	V_{GS}=-20V, V_{DS}=0V	--	--	100	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	V_{GS}=+20V, V_{DS}=0V	--	--	-100	nA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250μA	-1.1	-1.5	-2.0	V
$R_{DS(ON)1}$	Drain-to-Source On-Resistance	V_{GS}=-10V, I_D=-0.2A	--	1.5	2.5	Ω
$R_{DS(ON)2}$	Drain-to-Source On-Resistance	V_{GS}=-4.5V, I_D=-0.1A	--	2.0	4.0	Ω

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
C_{iss}	Input Capacitance	V_{GS} = 0V V_{DS} =-30V f = 1.0MHz	--	13.8	--	pF
C_{oss}	Output Capacitance		--	3.7	--	
C_{rss}	Reverse Transfer Capacitance		--	1.4	--	

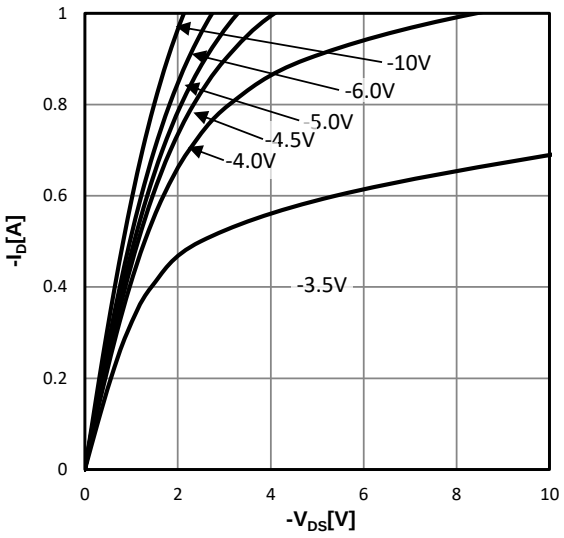
Resistive Switching Characteristics						
Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	I_D =-0.2A V_{DS} =-30V V_{GS} =-10V R_G =3.9Ω	--	6.0	--	ns
t_r	Rise Time		--	5.0	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	26	--	
t_f	Fall Time		--	14	--	
Q_g	Total Gate Charge	V_{GS} =-10V V_{DS} = -30V I_D =-0.2A	--	0.87	--	nC
Q_{gs}	Gate Source Charge		--	0.20	--	
Q_{gd}	Gate Drain Charge		--	0.35	--	

Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Value			Units
			Min.	Typ.	Max.	
I_S	Diode Forward Current	T_C =25 °C	--	--	-0.30	A
V_{SD}	Diode Forward Voltage	I_S=-0.2A, V_{GS}=0V	--	--	-1.2	V

a1：Repetitive rating; pulse width limited by maximum junction temperature

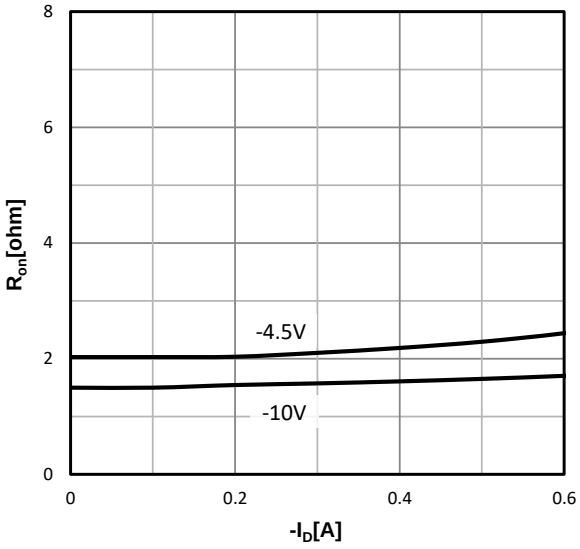
Characteristics Curve

Figure 1: Typ. output characteristics



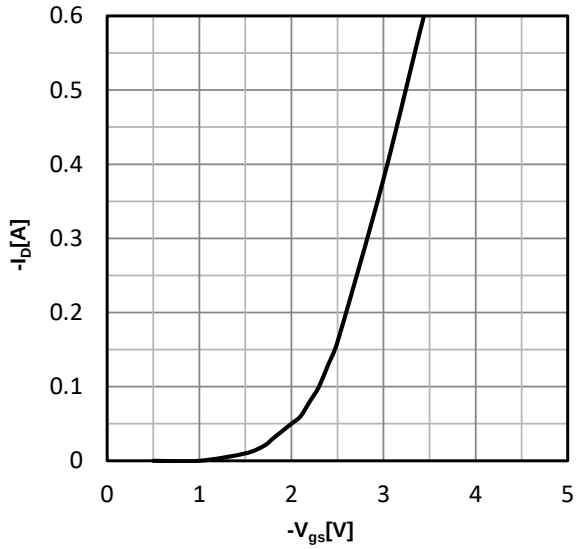
$I_D=f(V_{DS})$, T_j=25 °C; parameter: V_{GS}

Figure 2: Typ. drain-source on resistance



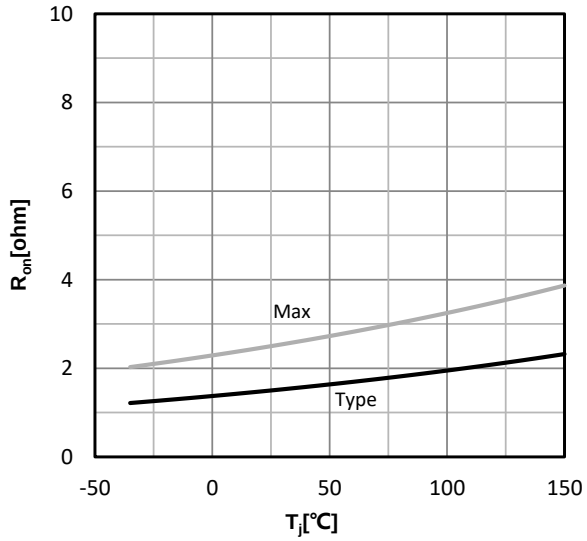
$R_{DS(on)}=f(I_D)$, T_j=25 °C; parameter: V_{GS}

Figure 3: Typ. transfer characteristics



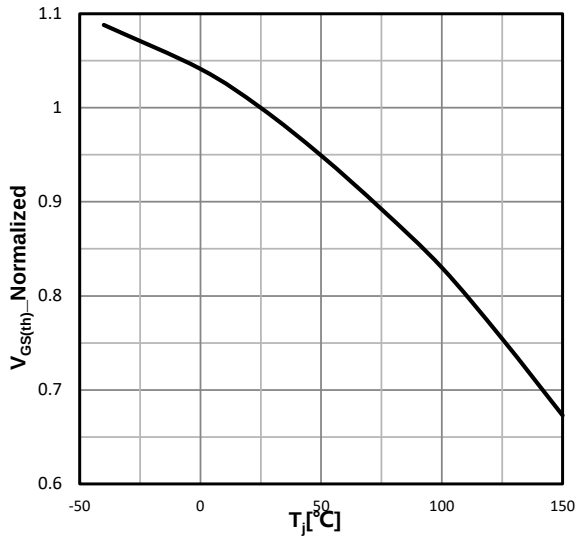
$I_D=f(V_{GS})$, $|V_{DS}|>2|I_D|R_{DS}(on)max$;

Figure 4: drain-source on resistance



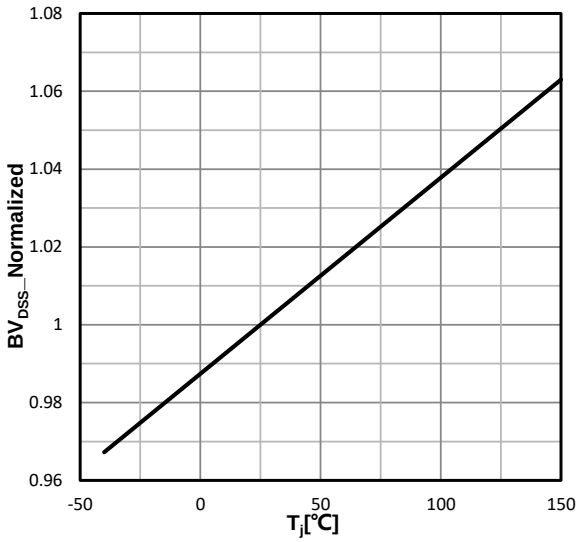
$R_{DS(on)}=f(T_j)$, I_D=-0.2A, V_{GS}=-10V;

Figure 5: Typ. gate threshold voltage



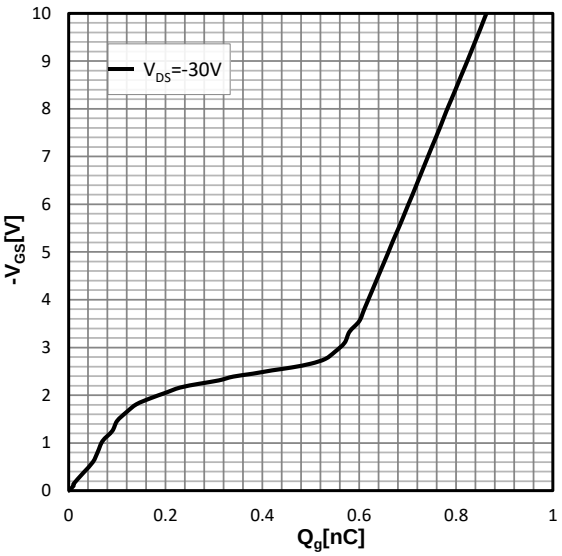
V_{GS}=f(T_j),I V_{GS}=$V_{DS,}$$I_D$=-250μA;

Figure 6: Drain-source breakdown voltage



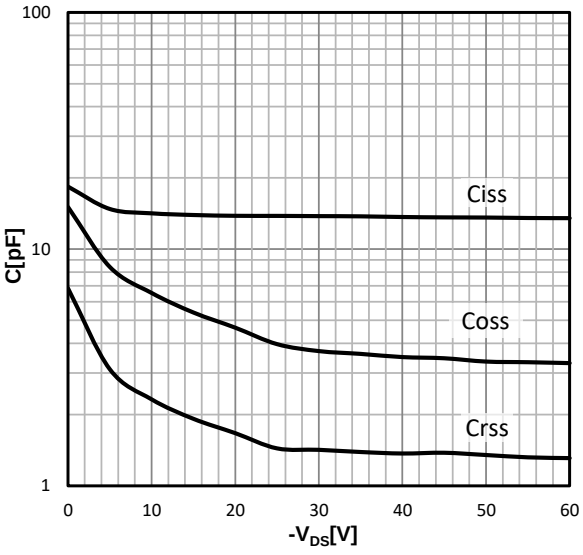
$V_{BR(DSS)}$=f(T_j); I_D=-250μA;

Figure 7: Typ. gate charge



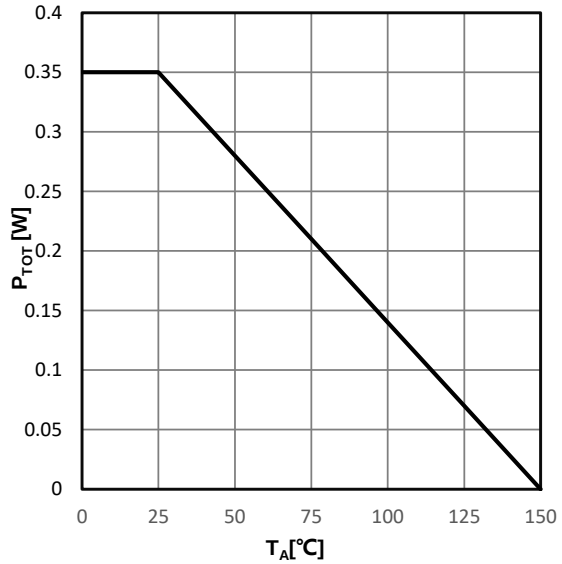
V_{GS}=f(Q_g), I_D=-0.2A, T_j=25 °C; parameter: V_{DS}

Figure 8: Typ. Capacitances



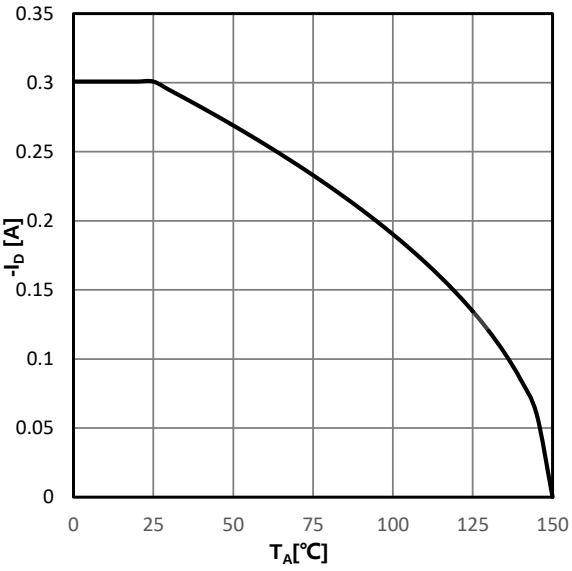
C=f(V_{DS}); V_{GS}=0V; f=1.0 MHz;

Figure 9: Power dissipation



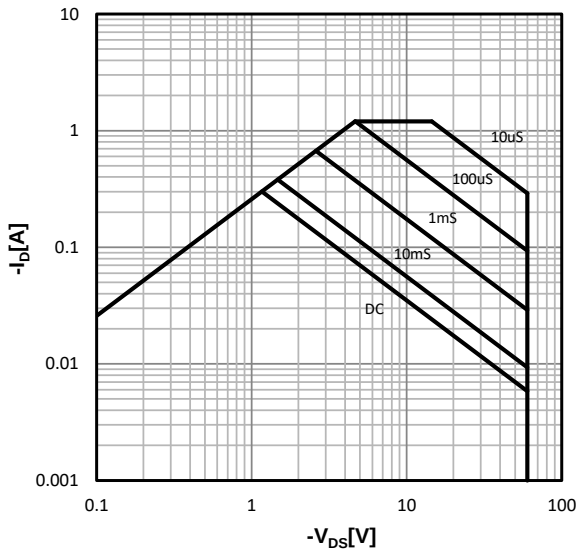
$P_{tot}=f(T_A)$;

Figure 10:Drain current



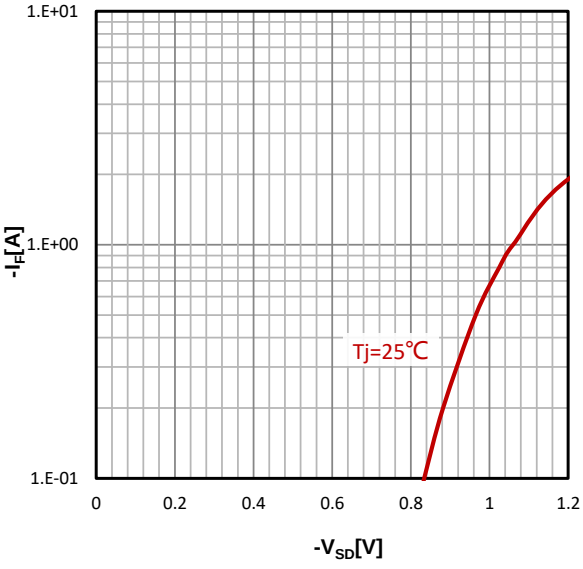
$I_D=f(T_A)$;

Figure 11: Safe operating area



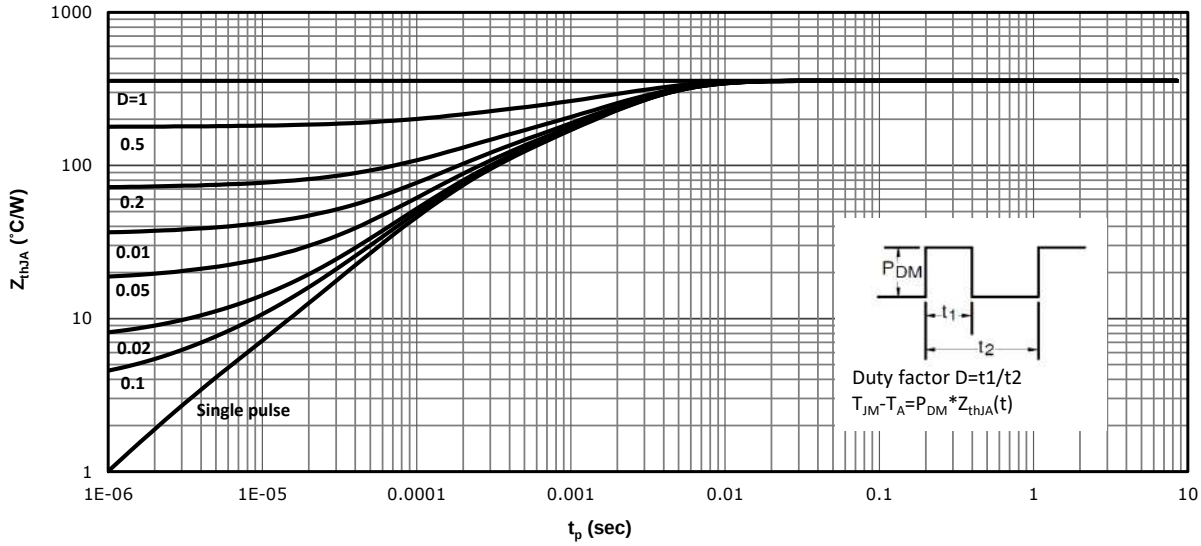
$I_D=f(V_{DS})$; T_A=25 °C; D=0; parameter: tp

Figure 12: Typ. forward characteristics



$I_F=f(V_{SD})$;

Figure 13: Max. Transient Thermal Impedance



$Z_{thJA}=f(t_p)$; parameter: D

Test Circuit & Waveform

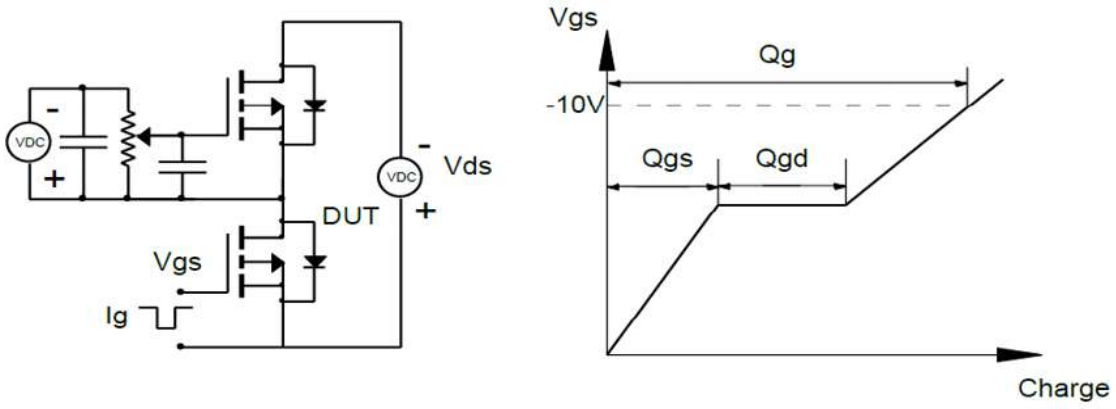


Figure 14: Gate Charge Test Circuit & Waveform

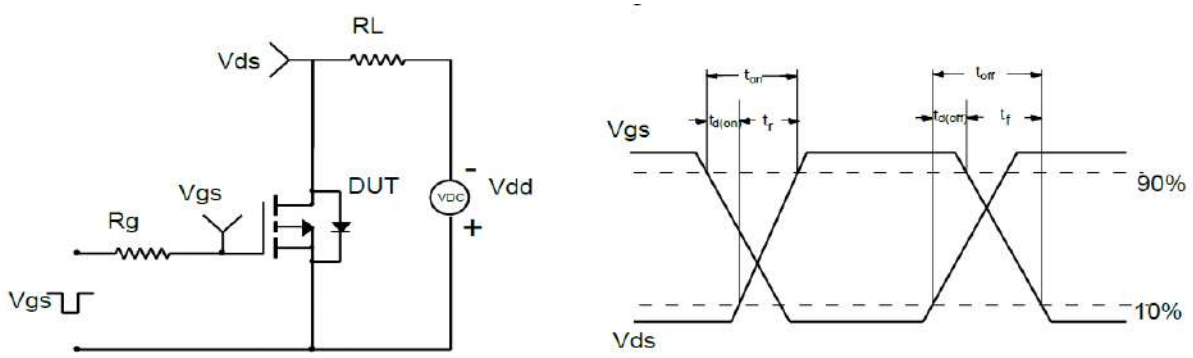


Figure 15: Resistive Switching Test Circuit & Waveforms

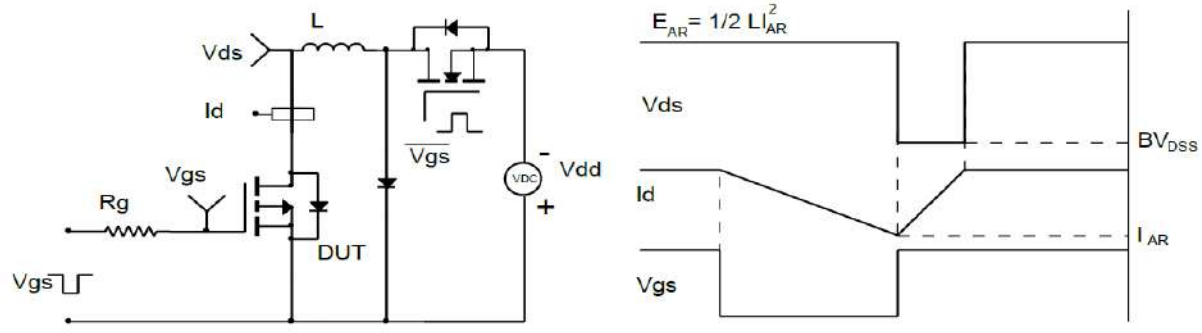
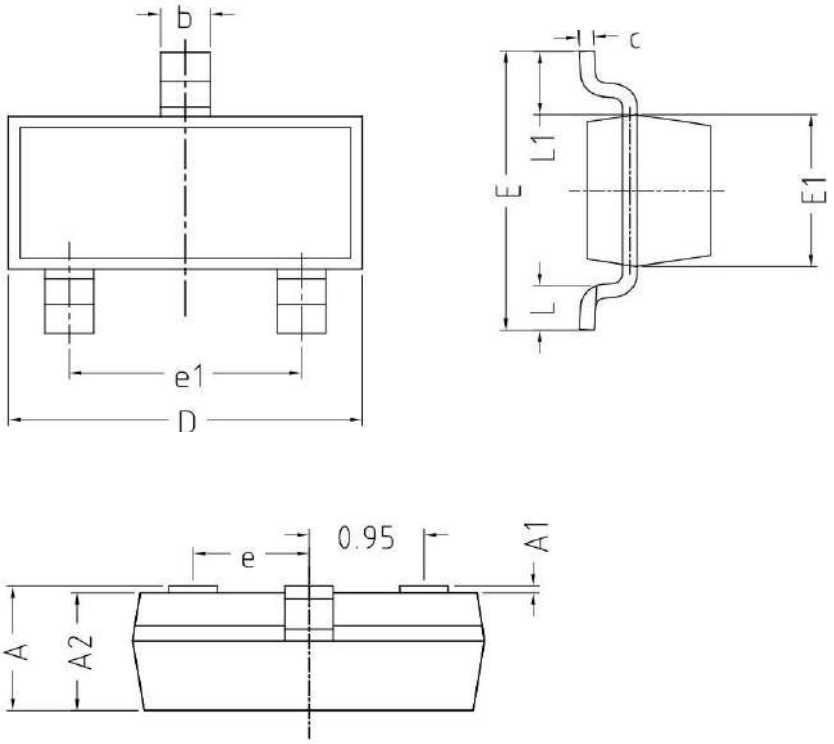


Figure 16: Unclamped Inductive Switching Test Circuit & Waveforms

Package Outline



COMMON IN DIMENSION (MM)			
Symbol	**Min.**	**Nom.**	**Max.**
A	0.900	1.050	1.150
A1	0.000	0.050	0.100
A2	0.900	1.000	1.050
b	0.300	0.400	0.500
C	0.100	0.130	0.200
D	2.800	2.900	3.000
E	2.250	2.400	2.550
E1	1.200	1.300	1.400
e	0.950 TYP		
e1	1.800	1.900	2.000
L	0.290	0.390	0.490
L1	0.550REF		