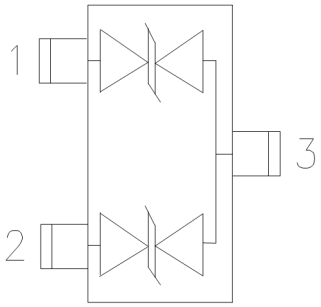
2-Line Bi-directional ESD Diode

Features

- 160W peak pulse power (8/20μs)
- Protects two bi-directional lines
- Ultra low leakage: nA level
- Operating voltage: 27V
- Low clamping voltage
- Complies with following standards:
  - IEC 61000-4-2 (ESD) immunity test
    - Air discharge: ±30kV
    - Contact discharge: ±30kV
  - IEC61000-4-4 (EFT) 40A (5/50ns)
  - IEC61000-4-5 (Lightning) 4A (8/20μs)
- RoHS Compliant
- AEC-Q101 qualified

Dimensions SOT-23

Pin Configuration



Applications

- Cellular Handsets and Accessories
- Notebooks and Handhelds
- Portable Instrumentation
- Set Top Box
- Industrial Controls
- Server and Desktop PC
- CAN BUS PROTECTION

Mechanical Characteristics

- Package: SOT-23
- Lead Finish: Lead Free
- UL Flammability Classification Rating 94V-0
- Quantity Per Reel:3,000pcs
- Reel Size:7inch
- Device Marking:SCH

Absolute Maximum Ratings(Tamb=25°C unless otherwise specified)

Parameter	Symbol	Value	Unit
Peak Pulse Power (8/20μs)	Ppk	160	W
ESD per IEC 61000−4−2 (Air) ESD per IEC 61000−4−2 (Contact)	VESD	±30 ±30	kV
Operating Temperature Range	TJ	−55 to +125	°C
Storage Temperature Range	Tstg	−55 to +150	°C

Electrical Characteristics(TA=25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}				27	V
Breakdown Voltage	V_{BR}	I_T = 1mA	28			V
Reverse Leakage Current	I_R	V_{RWM} = 27V			0.1	μA
Clamping Voltage	V_C	I_{PP} = 1A (8 x 20μs pulse)			33	V
Clamping Voltage	V_C	I_{PP} = 4A (8 x 20 μs pulse)			40	V
Junction Capacitance	C_J	VR = 0V, f = 1MHz		12		pF

Characteristic Curves

Figure 1. 8 x 20 μs Waveform

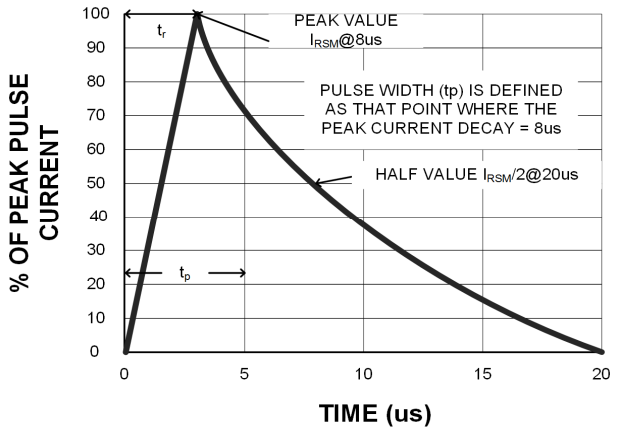


Figure 2. Power Derating Curve

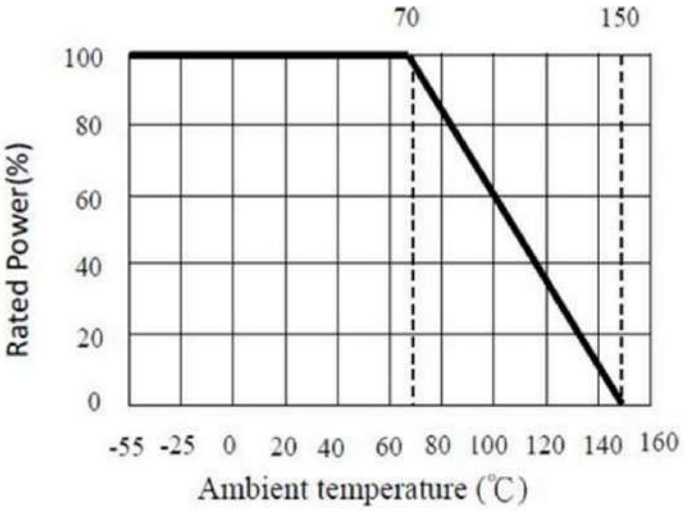


Figure 3. Clamping Voltage vs. Peak Pulse Current (tp=8/20 μs)

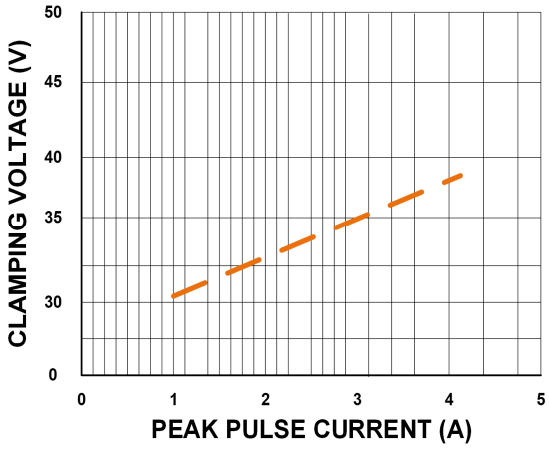


Figure 4. Typic Breakdown Voltage vs. Temperature

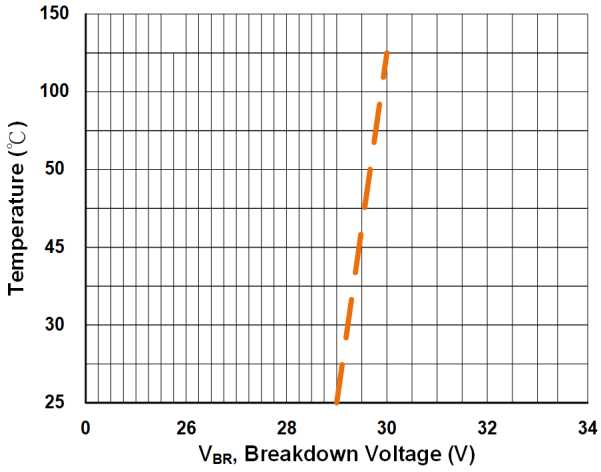


Figure 5. Typic Reverse Current vs. Temperature

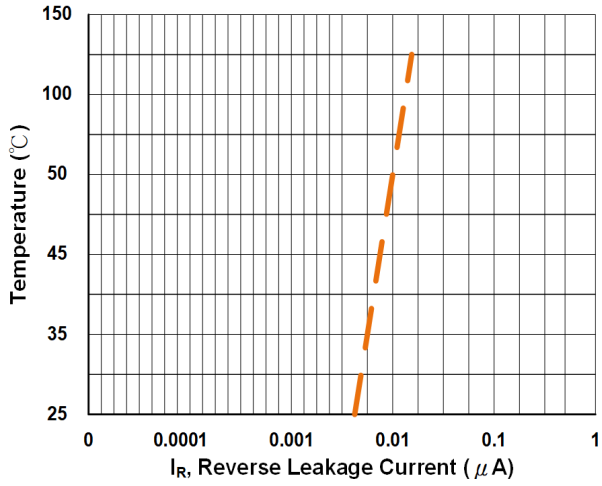
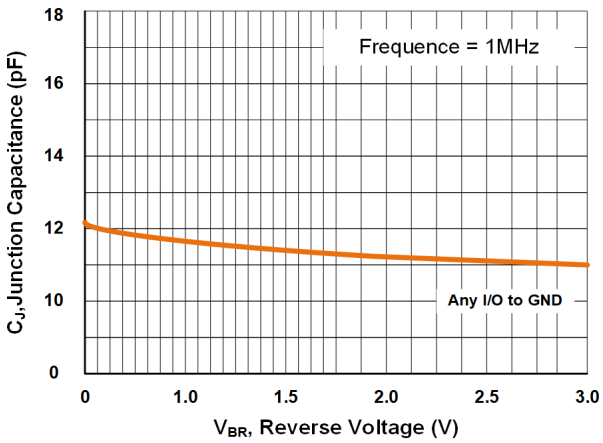


Figure 6. Typic Capacitance vs. Reverse Voltage



APPLICATION INFORMATION

Figure 7. Layout Guidelines

Steps must be taken for proper placement and signal trace routing of the ESD protection device in order to ensure the maximum ESD survivability and signal integrity for the application. Such steps are listed below.

1. Place the ESD protection device as close as possible to the I/O connector to reduce the ESD path to ground and improve the protection performance.

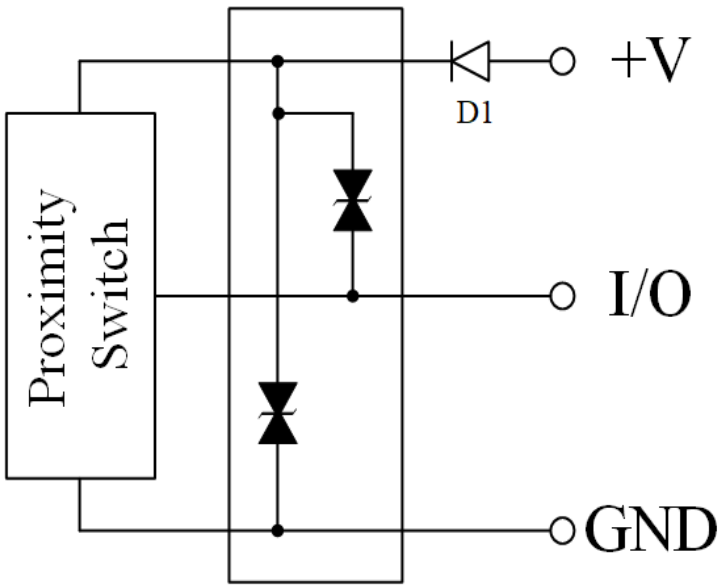
1.1. In USB 3.0/3.1 applications, the ESD protection device should be placed between the AC coupling capacitors and the I/O connector on the TX differential lanes as shown in below drawing In this configuration, no DC current can flow through the ESD protection device preventing any potential latch-up condition. For more information on latchup considerations, see below description on below drawing.

2. Make sure to use differential design methodology and impedance matching of all high speed signal traces.

2.1. Use curved traces when possible to avoid unwanted reflections.

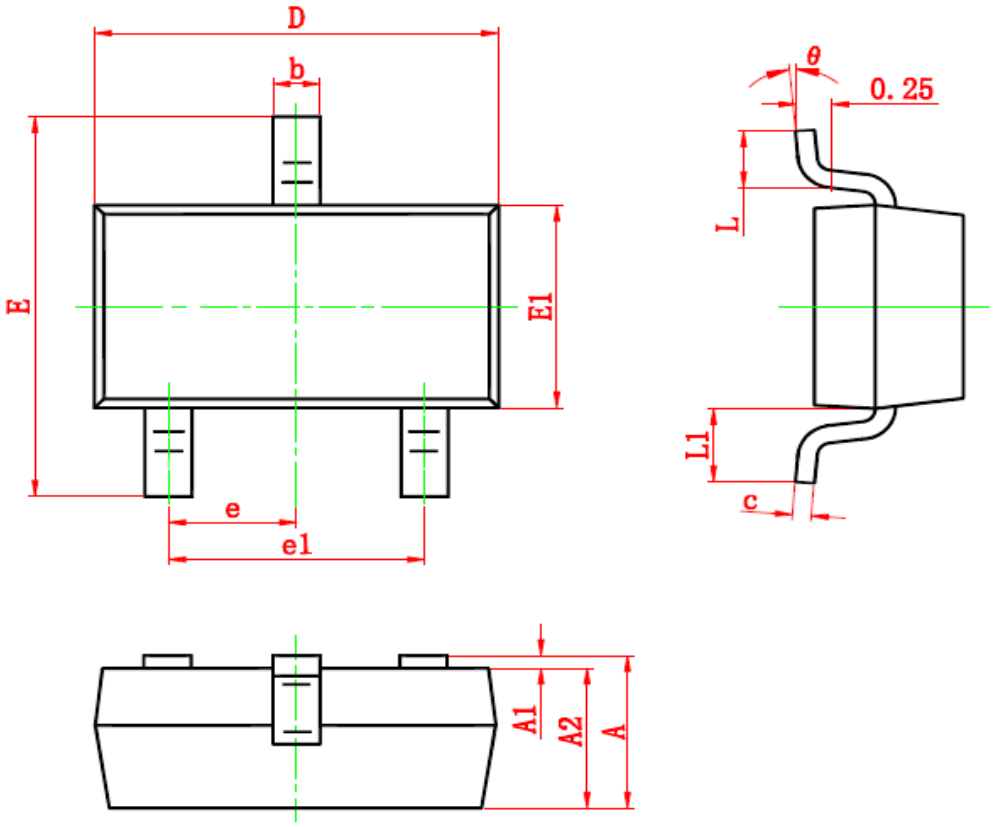
2.2. Keep the trace lengths equal between the positive and negative lines of the differential data lanes to avoid common mode noise generation and impedance mismatch.

2.3. Place grounds between high speed pairs and keep asmuch distance between pairs as possible to reduce crosstalk.



3-Wire Sensor
Circuit Protection

SOT-23 Package Outline & Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.900	1.150	0.035	0.045
A1	0.000	0.100	0.000	0.004
A2	0.900	1.050	0.035	0.041
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	2.250	2.550	0.089	0.100
E1	1.200	1.400	0.047	0.055
e	0.950 TYP.		0.037 TYP.	
e1	1.800	2.000	0.071	0.079
L	0.300	0.500	0.012	0.020
L1	0.550 REF.		0.022 REF.	
θ	0°	8°	0°	8°