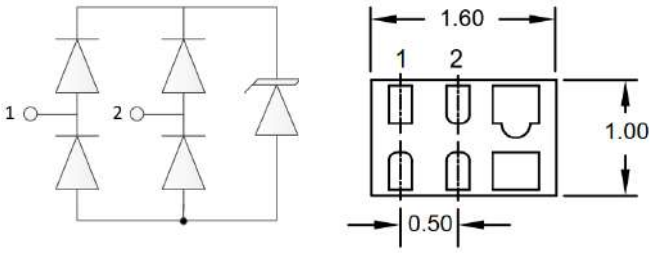
2-Line Ultra Low Capacitance TVS Diode Array

Features

- Ultra low capacitance: 0.4pF typical
- Ultra low leakage: nA level
- Operating voltage: 3.3V
- Low clamping voltage
- Complies with following standards:
  - – IEC 61000-4-2 (ESD) immunity test
    - Air discharge: ±30kV
    - Contact discharge: ±30kV
  - – IEC61000-4-5 (Lightning) 12A (8/20μs)
- Dynamic Resistance: 0.30 Ohms (Typ)
- Very small PCB area

Dimensions DFN1610N4

Pin Configuration



Applications

- 1G/2.5G/5G/10G Ethernet
- Integrated Magnetics / RJ-45 Connectors
- Central Office Equipment
- Industrial Equipment
- IP Camera

Mechanical Characteristics

- Package: DFN1610N4
- Pb-Free, Halogen Free, RoHS Compliant .
- Moisture Sensitivity: Level 3 per J-STD-020
- Quantity Per Reel:3,000pcs
- Reel Size:7inch
- Device Markin:3382P

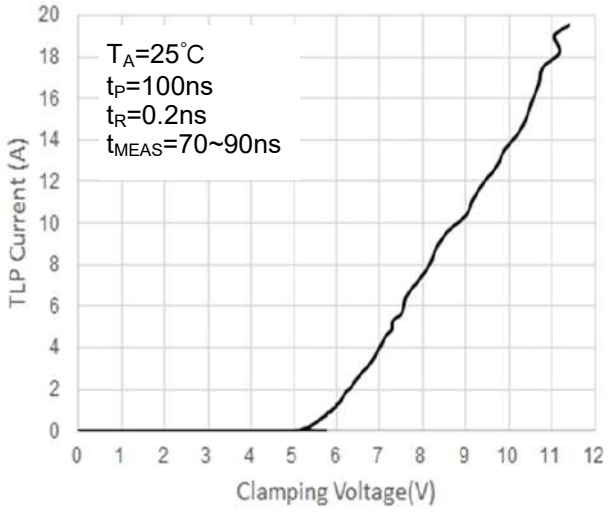
Absolute Maximum Ratings(Tamb=25°C unless otherwise specified)

Parameter	Symbol	Value	Unit
Peak Pulse Power (8/20μs)	Ppk	200	W
Peak Pulse Current (8/20μs)	IPP	12	A
ESD per IEC 61000−4−2 (Air) ESD per IEC 61000−4−2 (Contact)	VESD	±30 ±30	kV
Operating Temperature Range	TJ	−40 to +125	°C
Storage Temperature Range	Tstg	−55 to +150	°C

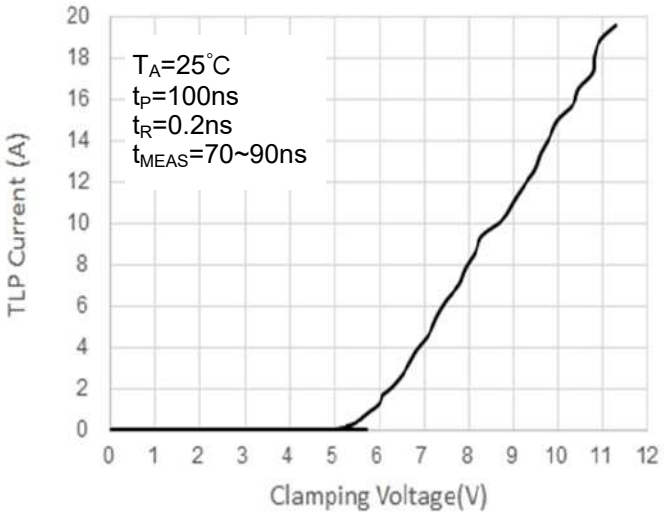
Electrical Characteristics (TA=25°C unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Reverse Working Voltage	V_{RWM}			3.3	V	Pin 1 to Pin 2
Breakdown Voltage	V_{BR1}	3.8	4.6	6.0	V	I_T = 2μA ,Pin 1 to Pin 2
	V_{BR2}	4.0	5.0	6.2	V	I_T = 50mA ,Pin 1 to Pin 2
Reverse Leakage Current	I_R			0.05	μA	V_{RWM} = 3.3V,Pin 1 to Pin 2
Clamping Voltage	V_C		12	16.5	V	I_{PP} = 12A ,Pin 1 to Pin 2 (8 x 20μs pulse)
ESD Clamping Voltage	V_C		7		V	IPP = 4A, tp = 0.2/100ns (TLP), Pin 1 to Pin 2
ESD Clamping Voltage	V_C		10.5		V	IPP = 16A, tp = 0.2/100ns (TLP), Pin 1 to Pin 2
Junction Capacitance	C_J		0.4	0.5	pF	VR = 0V, f = 1MHz,Pin 1 to Pin 2

Typical Performance Characteristics (T_A=25°C unless otherwise Specified)

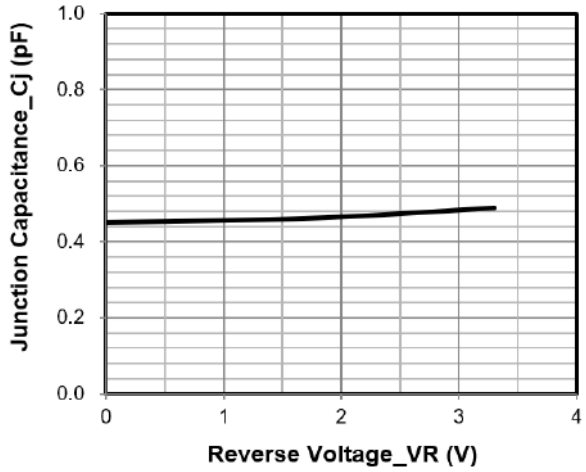


TLP IV Curve (Positive Pulse)

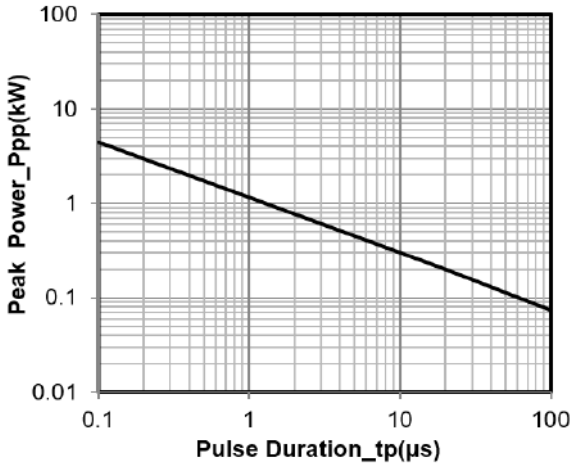


TLP IV Curve (Negative Pulse)

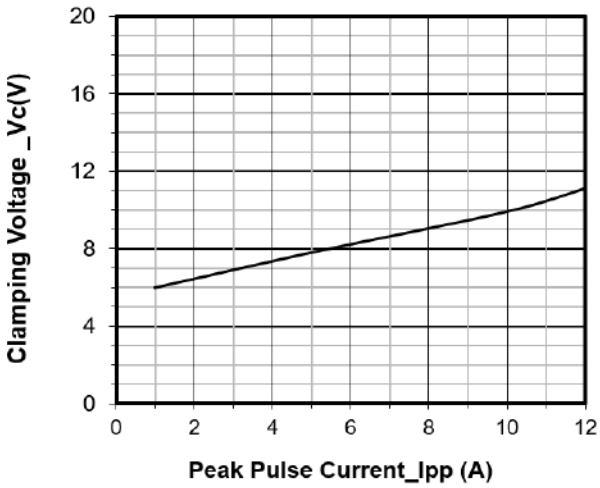
Typical Performance Characteristics (T_A=25°C unless otherwise Specified)



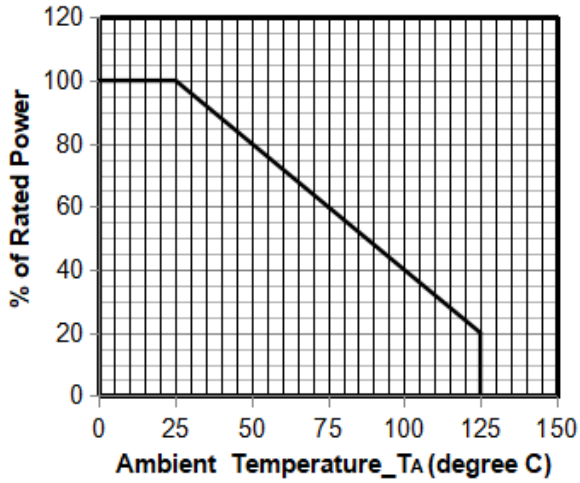
Junction Capacitance vs. Reverse Voltage



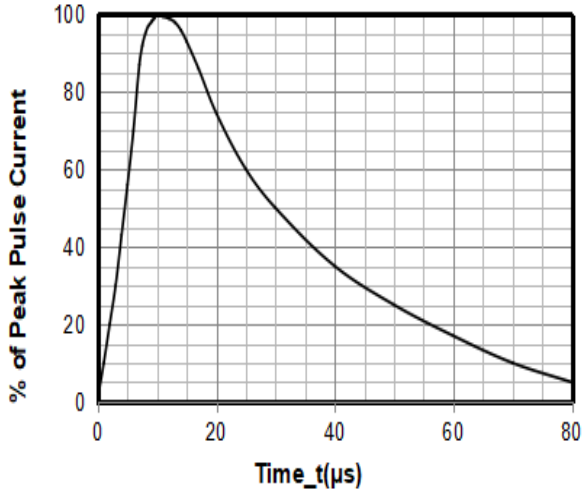
Peak Pulse Power vs. Pulse Time



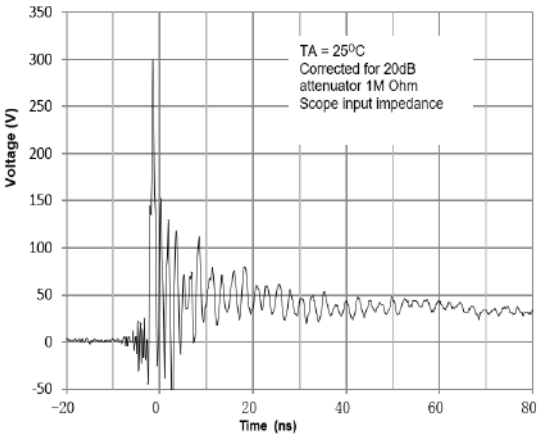
Clamping Voltage vs. Peak Pulse Current



Power Derating Curve



8 X 20μs Pulse Waveform



ESD Clamping Voltage

8 kV Contact per IEC61000−4−2

Application Information

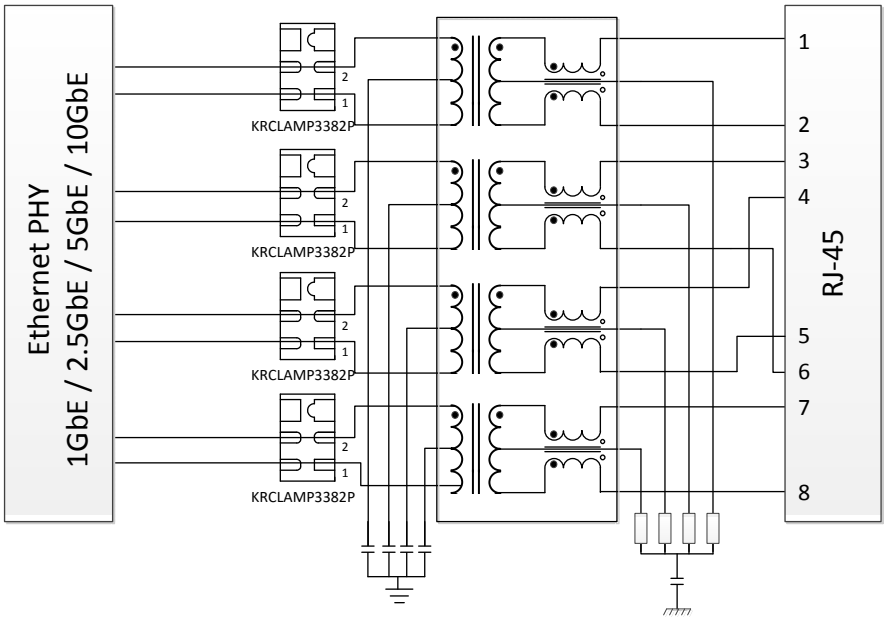
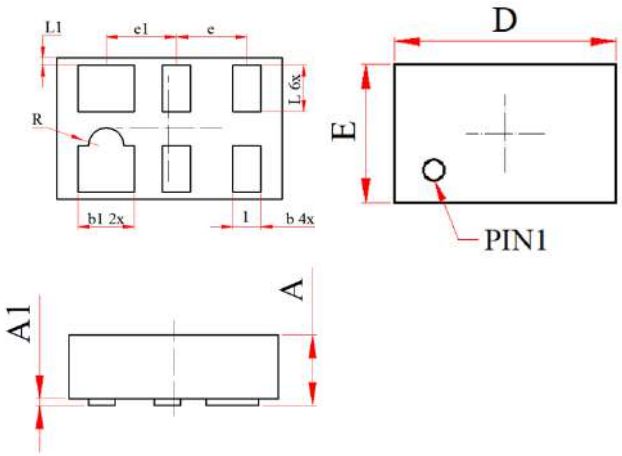


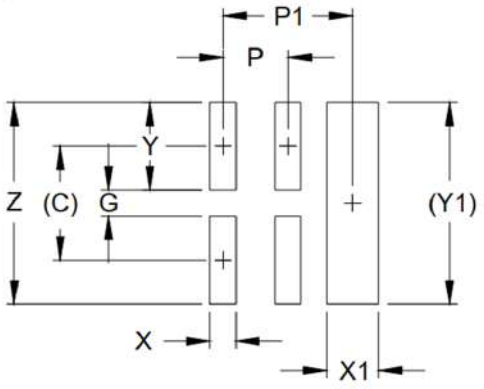
Figure 1 - Ethernet Protection Circuit

DFN1610N4 Package Outline Drawing



SYM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.450	--	0.550	0.018	--	0.022
A1	0.025	0.050	0.075	0.001	0.002	0.003
D	1.550	1.600	1.650	0.061	0.063	0.065
E	0.950	1.000	1.050	0.037	0.039	0.041
b	0.150	0.200	0.250	0.006	0.008	0.010
b1	0.350	0.400	0.450	0.014	0.016	0.018
L	0.300	0.350	0.400	0.012	0.014	0.016
L1	0.000	0.030	0.060	0.000	0.001	0.002
R	0.125 REF			0.005 REF		
e	0.500 BSC			0.020 BSC		
e1	0.500BSC			0.020 BSC		

Suggested Land Pattern



DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.034)	(0.87)
G	.007	0.19
P	.020	0.50
P1	.039	1.00
X	.008	0.20
X1	.016	0.40
Y	.027	0.68
Y1	(.061)	(1.55)
Z	.061	1.55