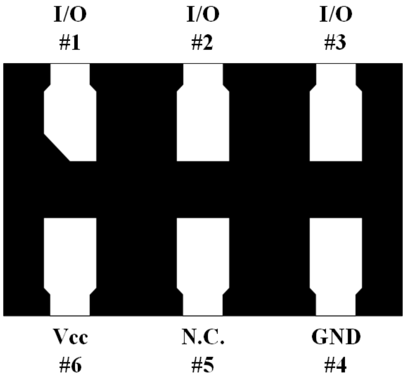
LOW CAPACITANCE TVS DIODE ARRAY

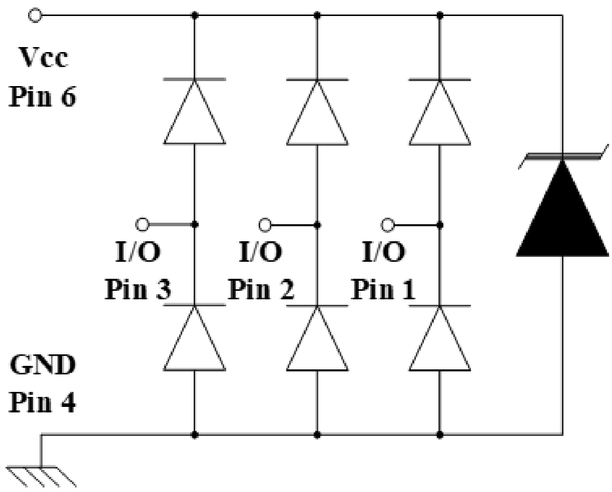
Features

- 56 Watts Peak Pulse Power per Line (tp=8/20 μs)
- Protects High Speed I/O Lines & V_{BUS}
- Low Clamping Voltage
- RoHS Compliant
- IEC61000-4-2 (ESD) ±15kV (air), ±10kV (contact)
- IEC61000-4-4 (EFT) 40A (5/50ηs)
- IEC61000-4-5 (LIGHTING) 3.5A (8/20 μs)

Dimensions DFN1510TP6



Pin Configuration



Applications

- Digital Visual Interface
- USB Ports
- LCD TV
- Serial ATA
- Firewire Ports
- Customer Premise Equipment
- HDMI Ports
- Infiniband Transceiver Protection

Mechanical Characteristics

- DFN1510TP6Package
- Molding Compound Flammability Rating : UL 94V-O
- Weight 3.0 Millgrams (Approximate)
- Reel Size : 7 inch
- Lead Finish : Lead Free
- Device Marking : UR53

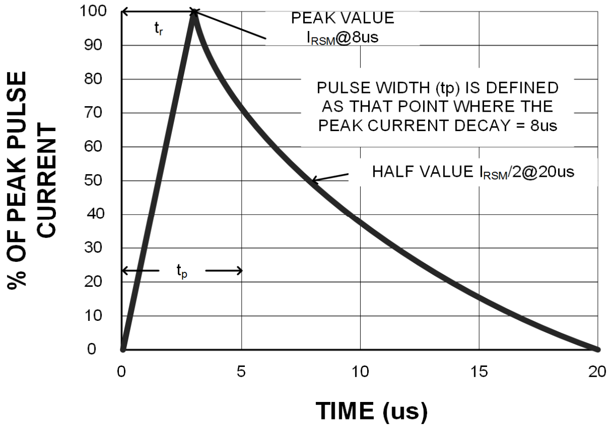
Absolute Maximum Ratings(Tamb=25°C unless otherwise specified)

PARAMETER	SYMBOL	VALUE	UNITS
Peak Pulse Power (tp=8/20μs waveform)	P_{PP}	56	Watts
Lead Soldering Temperature	T_L	260 (10 sec.)	℃
Operating Temperature Range	T_J	-40 ~ 125	℃
Storage Temperature Range	T_{STG}	-55 ~ 150	℃

Electrical Characteristics (TA=25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}				5	V
Breakdown Voltage	V_{BR}	I_T = 1mA	6			V
Reverse Leakage Current	I_R	V_{RWM} = 5V			0.1	µA
Clamping Voltage	V_C	I_{PP} = 1A (8 x 20 µs pulse)			9.8	V
Clamping Voltage	V_C	I_{PP} = 2A (8 x 20 µs pulse)			13	V
Clamping Voltage	V_C	I_{PP} = 3.5A (8 x 20 µs pulse)			16	V
Transmission Line Pulse	TLP	I_{OUT} = 1A		8.5		V
Transmission Line Pulse	TLP	I_{OUT} = 2A		11		V
Transmission Line Pulse	TLP	I_{OUT} = 5A		14		V
Junction Capacitance	C_J	V_R = 0V, f = 1MHz (I/O to I/O)		0.4		pF
Junction Capacitance	C_J	V_R = 0V, f = 1MHz (I/O to GND)		0.8		pF

TYPIC CHARACTERISTICS



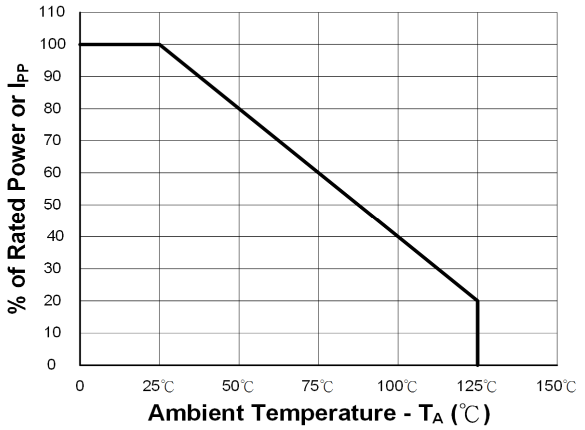


Figure 3. Clamping Voltage vs. Peak Pulse Current (TLP)

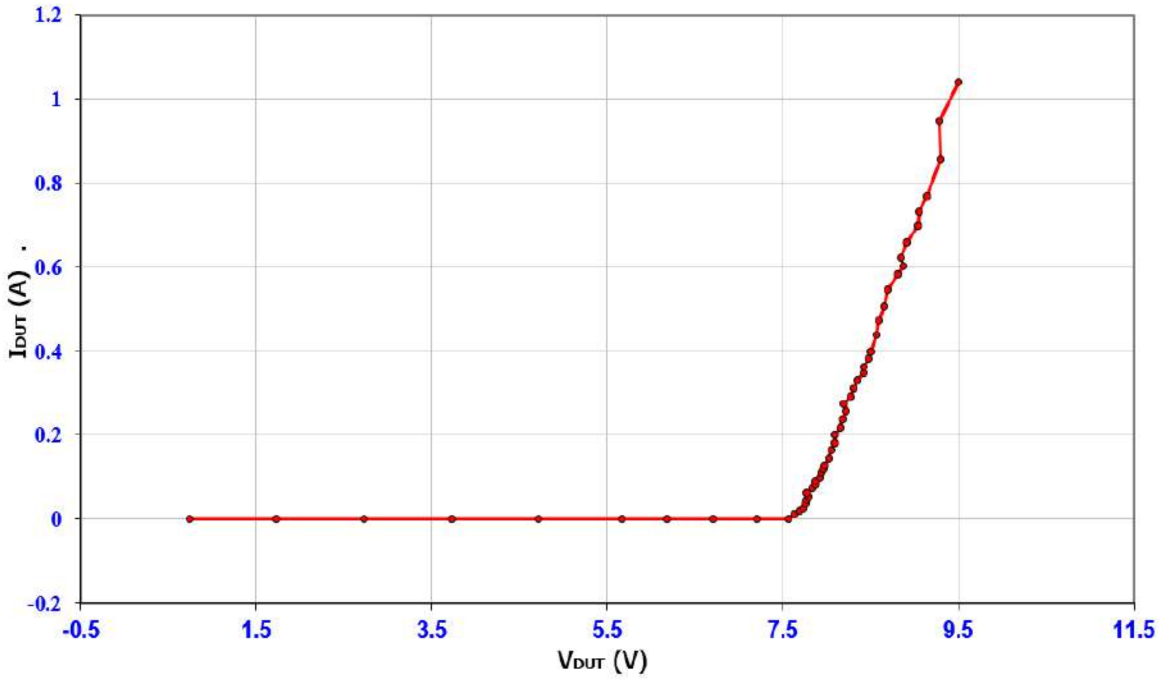


Figure 4. Typic Breakdown Voltage vs. Temperature

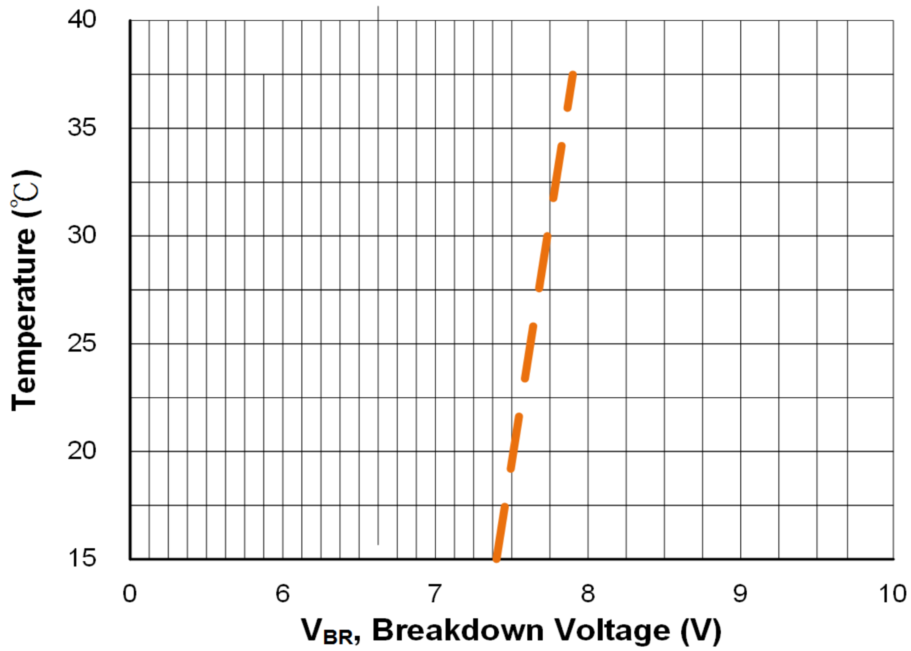


Figure 5. Typic Reverse Current vs. Temperature

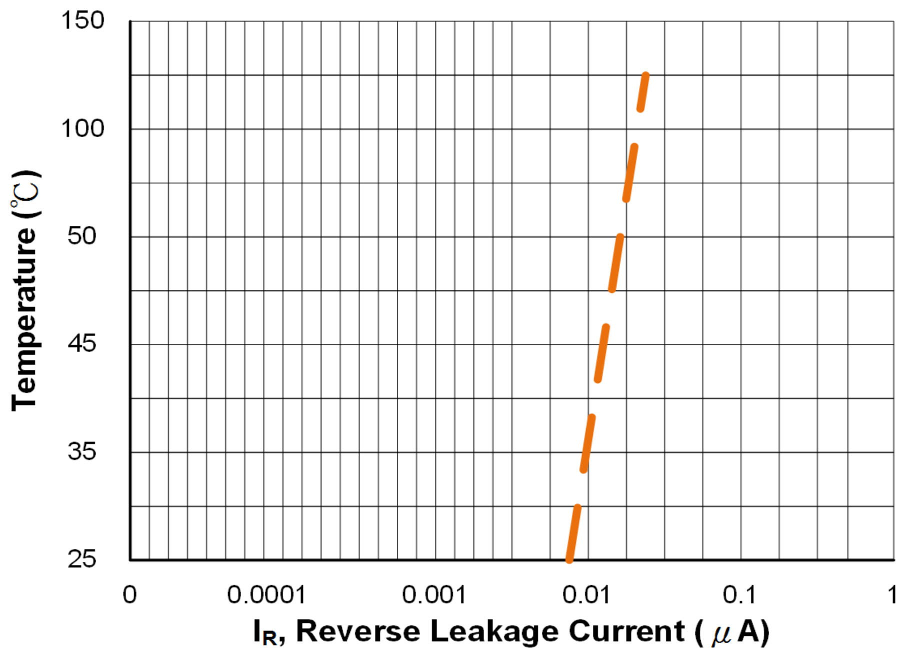


Figure 6. Typic Capacitance vs. Reverse Voltage

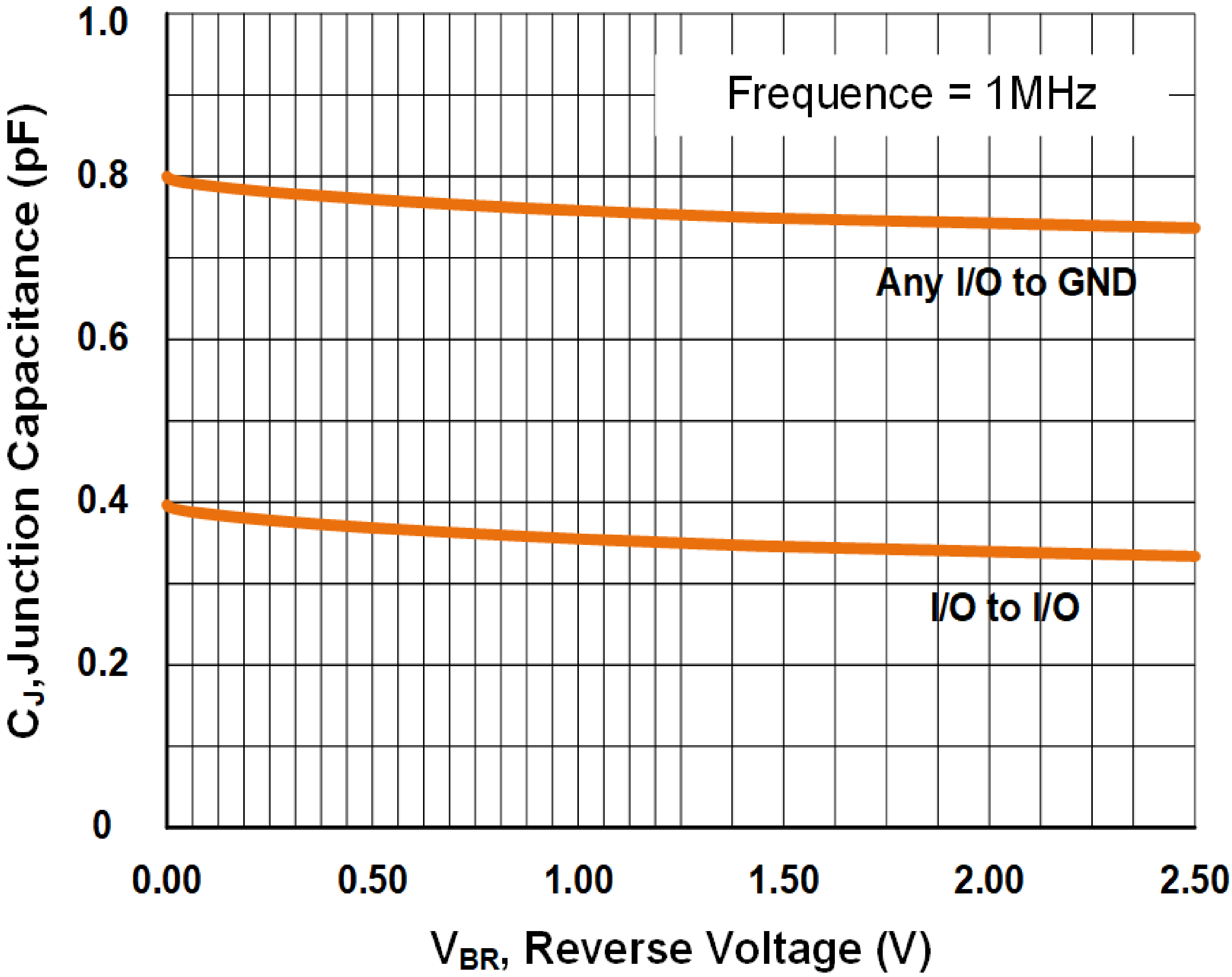
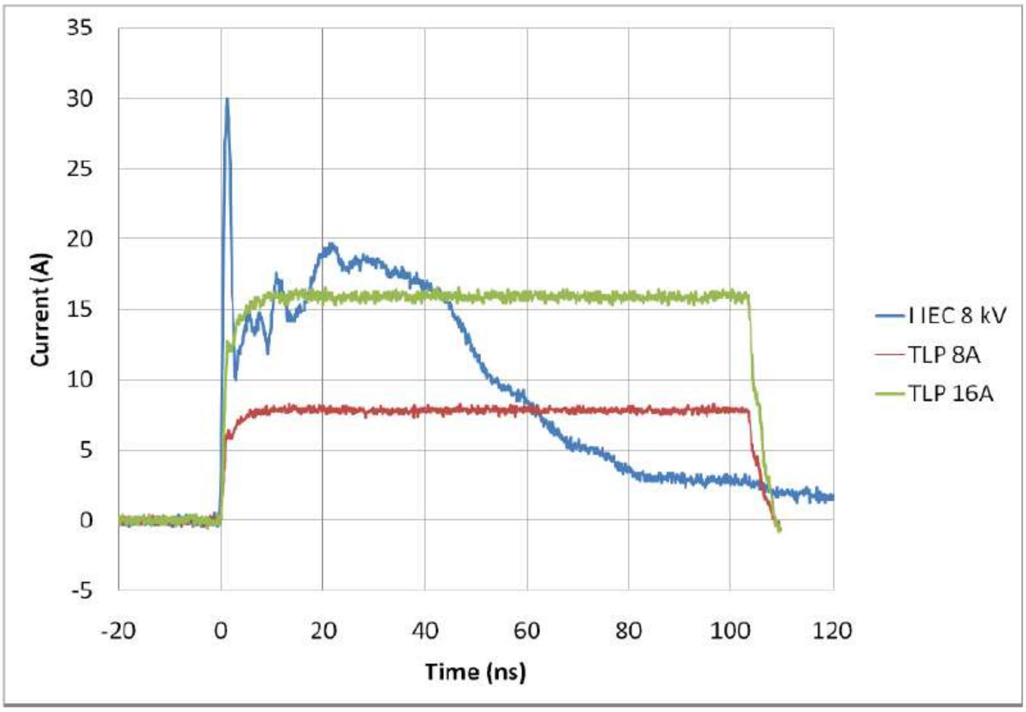


Figure 7. Transmission Line Pulse (TLP)

Transmission Line Pulse (TLP) is a measurement technique used in the Electrostatic Discharge (ESD) arena to characterize performance attributes of devices under ESD stresses. TLP is able to obtain current versus voltage (I−V) curves in which each data point is obtained with a 100 ns long pulse, with currents up to 40 A. TLP was first used in the ESD field to study human body model (HBM) in integrated circuits, but it is an equally valid tool in the field of system level ESD. The applicability of TLP to system level ESD is illustrated in Figure 1, which compares an 8 kV IEC 61000−4−2 current waveform with TLP current pulses of 8 and 16 A. The current levels and time duration for the pulses are similar and the initial rise time for the TLP pulse is comparable to the rise time of the IEC 61000−4−2's initial current spike. This application note will give a basic introduction to TLP measurements and explain the datasheet parameters extracted from TLP for SDI Technology's protection products.



Comparison Between 8 kV IEC 61000−4−2 and 8 A and 16 A TLP Waveforms

Comparison of a CurrentWaveform of IEC 61000−4−2with TLP Pulses at 8 and 16 A.
The IEC 61000−4−2 ESD waveforms is true to the Standard and is shown here as captured on an oscilloscope.
The points A, B, and C show the points on the aveforms specified in IEC 61000−4−2.
Transmission Line Pulse (TLP) Version.

Figure 8. Eye diagram on HDMI 1.4, USB 2.0 and

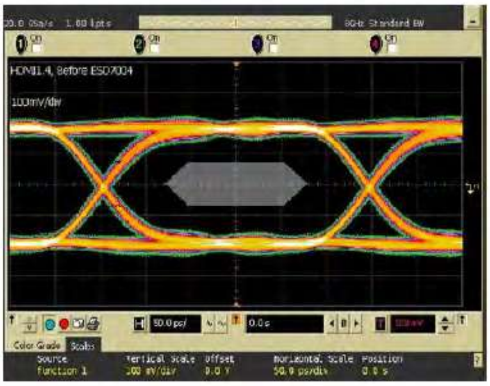


Fig. 8.1. @HDMI 1.4 mask at 3.4 Gbps per channel (Without Component)

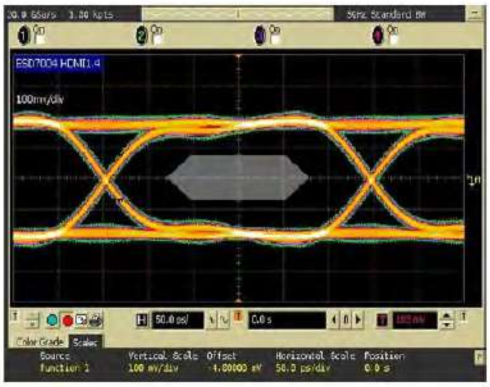


Fig. 8.2. @HDMI 1.4 mask at 3.4 Gbps per channel (With Component)

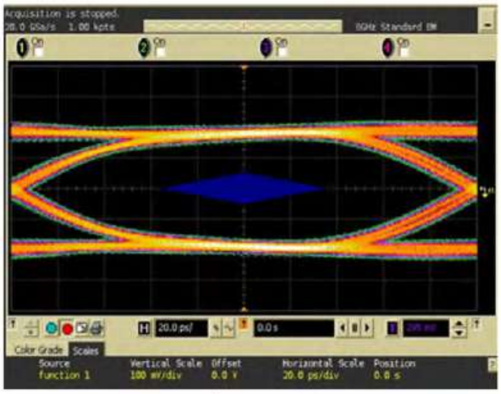


Fig. 8.3. @USB 2.0 mask at 3.2 Gbps per channel (Without Component)

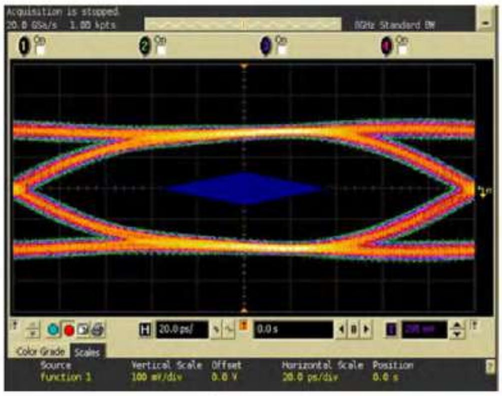


Fig. 8.4. @USB 2.0 mask at 3.2 Gbps per channel (With Component)

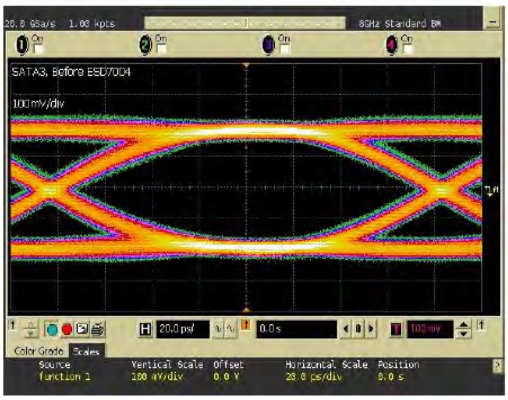


Fig. 8.5. @ESATA 2.0 mask at 3.8 Gbps per channel (Without Component)

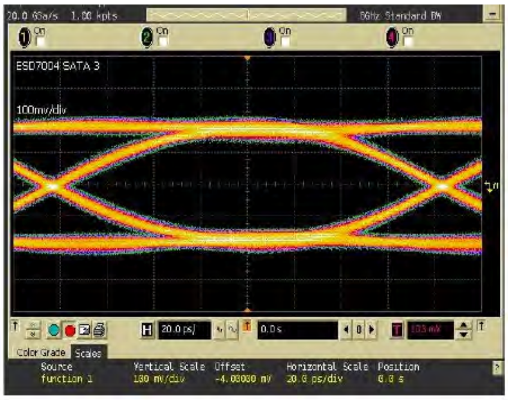


Fig. 8.6. @ESATA 2.0 mask at 3.8 Gbps per channel (With Component)

Figure 10. Layout Guidelines

Steps must be taken for proper placement and signal trace routing of the ESD protection device in order to ensure the maximum ESD survivability and signal integrity for the application. Such steps are listed below.

1. Place the ESD protection device as close as possible to the I/O connector to reduce the ESD path to ground and improve the protection performance.

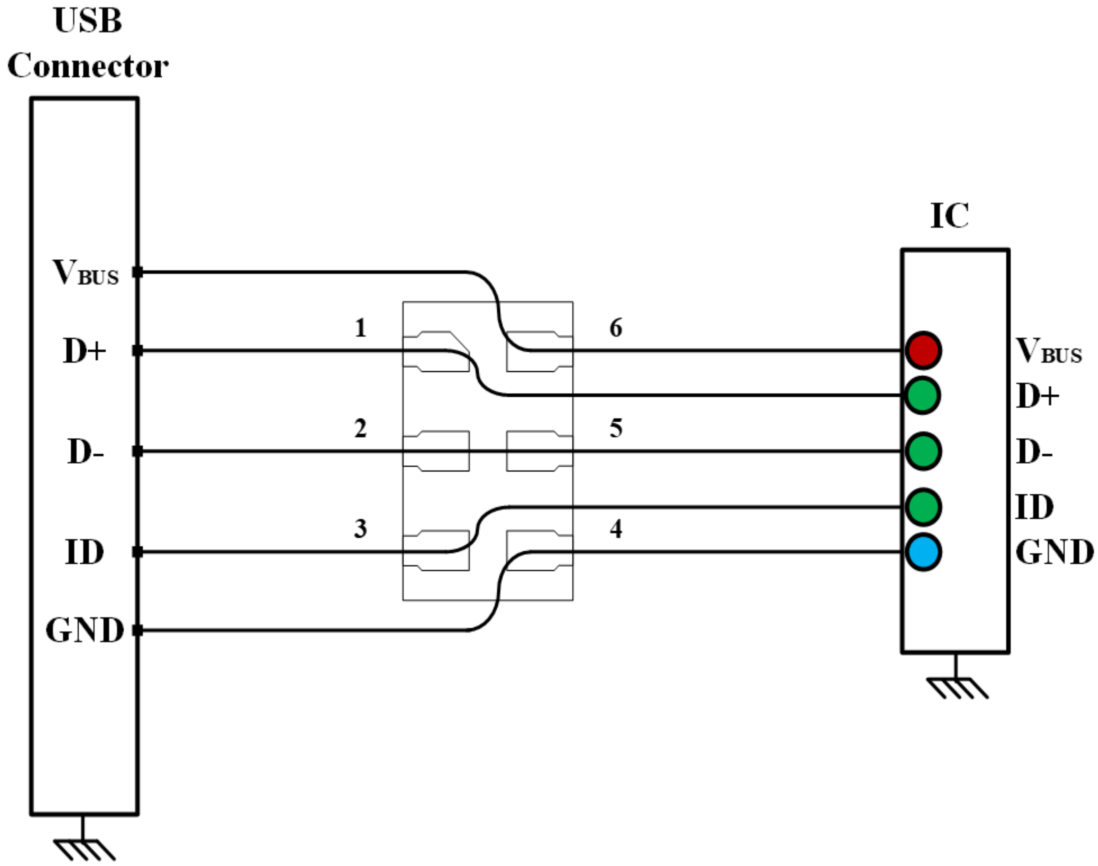
1.1. In USB 2.0 applications, the ESD protection device should be placed between the AC coupling capacitors and the I/O connector on the TX differential lanes as shown in below drawing In this configuration, no DC current can flow through the ESD protection device preventing any potential latch-up condition. For more information on latchup considerations, see below description on below drawing.

2. Make sure to use differential design methodology and impedance matching of all high speed signal traces.

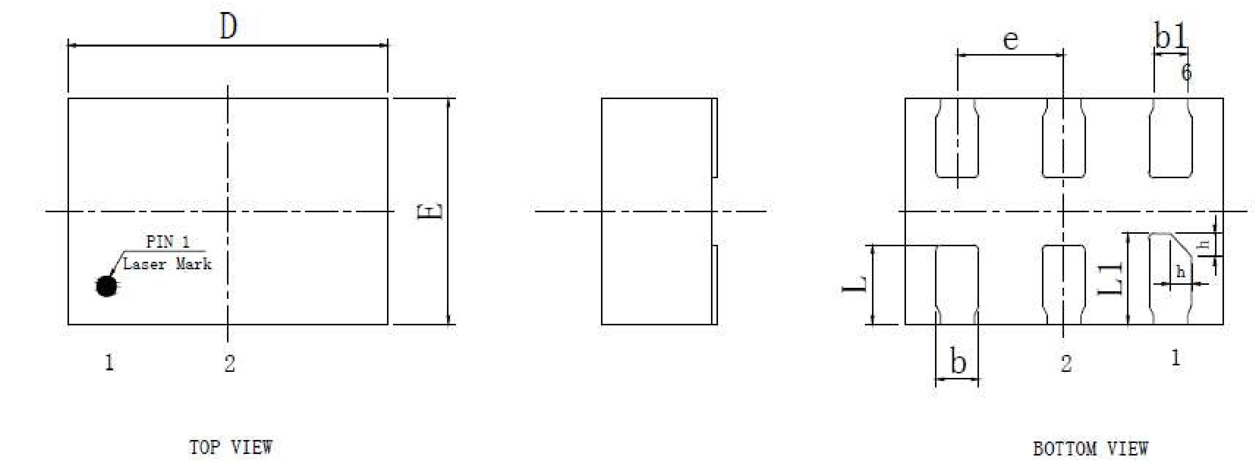
2.1. Use curved traces when possible to avoid unwanted reflections.

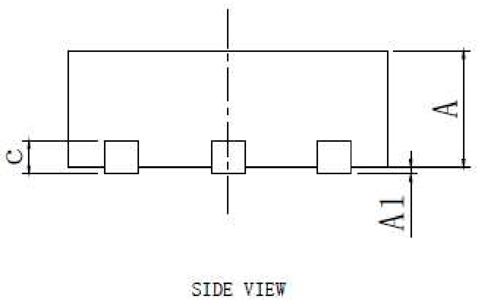
2.2. Keep the trace lengths equal between the positive and negative lines of the differential data lanes to avoid common mode noise generation and impedance mismatch.

2.3. Place grounds between high speed pairs and keep asmuch distance between pairs as possible to reduce crosstalk.



DFN1510TP6 PACKAGE OUTLINE & DIMENSIONS





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0. 50	0. 55	0. 60
A1	0	0. 02	0. 05
b	0. 15	0.20	0. 25
b1	0.16REF		
c	0.15REF		
D	1. 40	1. 50	1. 60
E	0. 90	1. 00	1. 10
e	0. 50BSC		
L	0. 30	0.35	0. 40
L1	0. 35	0.40	0. 45
h	0. 05	0. 10	0. 15