

KWULC0521CDN

ULTRA LOW CAPACITANCE TVS DIODE ARRAY

Features:

- 51 Watts Peak Pulse Power per Line (tp= $8/20\mu$ s)
- Protects One Bidirectional I/O Line
- ♦ Low Clamping Voltage
- RoHS Compliant

Applications:

- Cellular Handsets & Accessories
- ♦ Keypads, Side Keys, Audio Ports
- Portable Instrumentation'
- ♦ Notebooks, Desktops, and Servers
- Digital Lines
- ♦ Tablet PC

MECHANICAL CHARACTERISTICS

- ♦ DFN1006DN Package
- ♦ Molding Compound Flammability Rating : UL 94V-O
- Weight 0.5 Millgrams (Approximate)
- ♦ Reel Size : 7 inch
- ♦ Lead Finish : Lead Free

IEC COMPATIBILITY

- ◆ IEC61000-4-2 (ESD) ±17kV (air), ±15kV (contact)
- ♦ IEC61000-4-4 (EFT) 40A (5/50ηs)
- ◆ IEC61000-4-5 (LIGHTING) 3.4A (8/20µ s)

DFN1006DN Configuration



Typic Application Schematic





DEVICE CHARACTERISTICS

MAXIMUM RATINGS (@ 25°C Unless Otherwise Specified)

PARAMETER	SYMBOL	VALUE	UNITS
Peak Pulse Power (tp=8/20µs waveform)	P_{PP}	51	Watts
Lead Soldering Temperature	T _L	260 (10 sec.)	°C
Operating Temperature Range	T_{J}	-40 ~ 125	°C
Storage Temperature Range	T _{STG}	-55 ~ 150	°C

ELECTRICAL CHARACTERISTICS PER LINE

PART NUMBER	DEVICE MARKING	V _{RWM} (V) (max.)	V _B (V) (min.)	I _T (mA	V _C (@1A) (max.)	V _C (@2A) (max.)	V _C (@3.4A) (A)	I _R (µ A) (max.)	C _T (pF) (typ.)
KWULC0521CDN	НА	5	6	1	9.8	11.8	15	0.1	0.24





Figure 3. Clamping Voltage vs. Peak Pulse Current (tp=8/20µ s)



Figure 1. 8 x 20µ s Waveform

Figure 2.Power Derating Curve





Figure 4. Typic Breakdown Voltage vs. Temperature

Figure 5. Typic Reverse Current vs. Temperature











Figure 8. Eye diagram on HDMI 2.0, USB 3.0 and USB 3.1





APPLICATION INFORMATION

Figure 9. Layout Guidelines

Steps must be taken for proper placement and signal trace routing of the ESD protection device in order to ensure the maximum ESD survivability and signal integrity for the application. Such steps are listed below.

1. Place the ESD protection device as close as possible to the I/O connector to reduce the ESD path to ground and improve the protection performance.

1.1. In USB 3.0/3.1 applications, the ESD protection device should be placed between the AC coupling capacitors and the I/O connector on the TX differential lanes as shown in below drawing In this configuration, no DC current can flow through the ESD protection device preventing any potential latch-up condition. For more information on latchup considerations, see below description on below drawing.

2. Make sure to use differential design methodology and impedance matching of all high speed signal traces.

2.1. Use curved traces when possible to avoid unwanted reflections.

2.2. Keep the trace lengths equal between the positive and negative lines of the differential data lanes to avoid common mode noise generation and impedance mismatch.

2.3. Place grounds between high speed pairs and keep asmuch distance between pairs as possible to reduce crosstalk.



Fig. 9.1. High Spped I/O Layout Diagram

DFN1006DN PACKAGE OUTLINE & DIMENSIONS





BOTTOM VIEW

SYMPOL	MILLIMETER					
SIMBOL	MIN NOM		MAX			
А	0.45	0.50	0.55			
A1	0	0.02	0.05			
b	0.45	0.50	0.55			
с	0.12	0.15	0.18			
D	0.95	1.00	1.05			
е	0.65 BSC					
Е	0.55	0.60	0.65			
L	0.20	0.25	0.30			
L1	0.05REF					
h	0.07	0.12	0.17			

