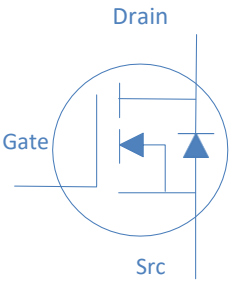
30V N-Ch Power MOSFET

DFN5x6

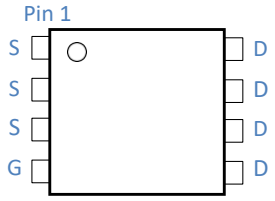
Features:

- ◇ Optimized for high speed switching, Logic Level
- ◇ Enhanced Body diode dv/dt capability
- ◇ Enhanced Avalanche Ruggedness
- ◇ 100% UIS Tested, 100% Rg Tested
- ◇ Lead Free, Halogen Free



Application:

- ◇ Synchronous Rectification in SMPS
- ◇ Hard Switching and High Speed Circuit
- ◇ Power Tools
- ◇ UPS
- ◇ Motor Control



Part Number	Package	Marking
KPRTN010N03P	DFN5x6	TN010N03P

V_{DS}		30	V
$R_{DS(on),max}$	V_{GS}=10V	1.0	mΩ
$R_{DS(on),max}$	V_{GS}=4.5V	1.4	mΩ
I_D		254	A

Absolute Maximum Ratings at T_j=25℃ (unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	I_D	T_C=25℃	254	A
		T_C=100℃	160	
Drain to Source Voltage	V_{DS}	-	30	V
Gate to Source Voltage	V_{GS}	-	±20	V
Pulsed Drain Current	I_{DM}	-	400	A
Avalanche Energy, Single Pulse	E_{AS}	L=0.3mH, T_C=25℃	375	mJ
Power Dissipation	P_D	T_C=25℃	96	W
Operating and Storage Temperature	T_J, T_{stg}	-	-55 to150	℃

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Case	$R_{\theta JC}$	1.3	℃/W
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	50	℃/W

Electrical Characteristics at T_j=25℃ (unless otherwise specified)

Static Characteristics

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=250μA	30	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=250μA	1	1.5	2	
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS}=0V, V_{DS}=24V, T_j=25℃	-	-	1	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Drain to Source on Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=20A	-	0.85	1	mΩ
		V_{GS}=4.5V, I_D=15A	-	1.1	1.4	mΩ
Transconductance	g_{fs}	V_{DS}=5V, I_D=10A	-	54	-	S
Gate Resistance	R_G	V_{GS}=0V, V_{DS} Open, f=1MHz	-	4	-	Ω

Dynamic Characteristics

Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=15V, f=1MHz	-	6545	-	pF
Output Capacitance	C_{oss}		-	996	-	
Reverse Transfer Capacitance	C_{rss}		-	772	-	
Total Gate Charge (10V)	Q_g (10V)	V_{DD}=15V, I_D=20A, V_{GS}=10V	-	175.7	-	nC
Total Gate Charge (10V)	Q_g (4.5V)		-	84	-	
Gate to Source Charge	Q_{gs}		-	30.6	-	
Gate to Drain (Miller) Charge	Q_{gd}		-	30	-	
Turn on Delay Time	$t_{d(on)}$	V_{DD}=15V, I_D=1A, V_{GS}=10V, R_G=6Ω,	-	14	-	ns
Rise time	t_r		-	24.1	-	
Turn off Delay Time	$t_{d(off)}$		-	330	-	
Fall Time	t_f		-	133.5	-	

Reverse Diode Characteristics

Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_F=10A	-	0.7	1.1	V
Reverse Recovery Time	t_{rr}	I_F=10A, V_R=15V,dI_F/dt=100A/μs	-	36.9	-	ns
Reverse Recovery Charge	Q_{rr}		-	35.6	-	nC

Fig 1. Typical Output Characteristics

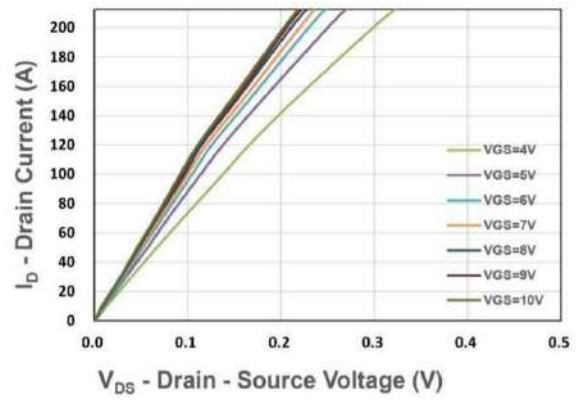


Figure 2. On-Resistance vs. Gate-Source Voltage

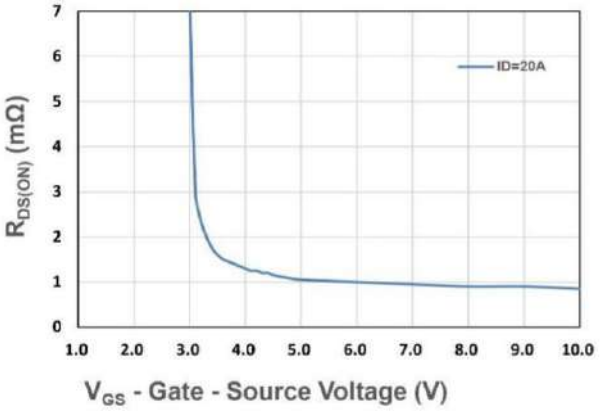


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

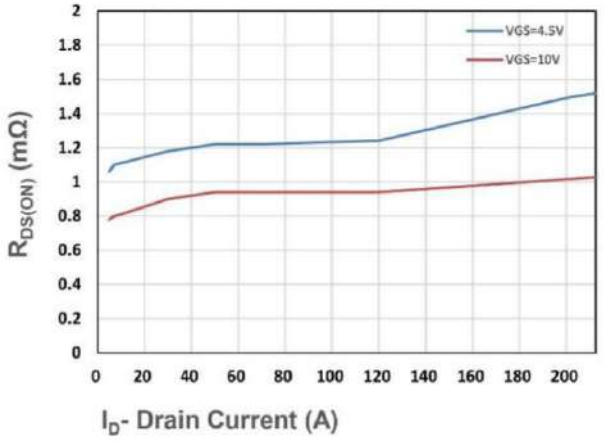


Figure 4. Normalized On-Resistance vs. Junction Temperature

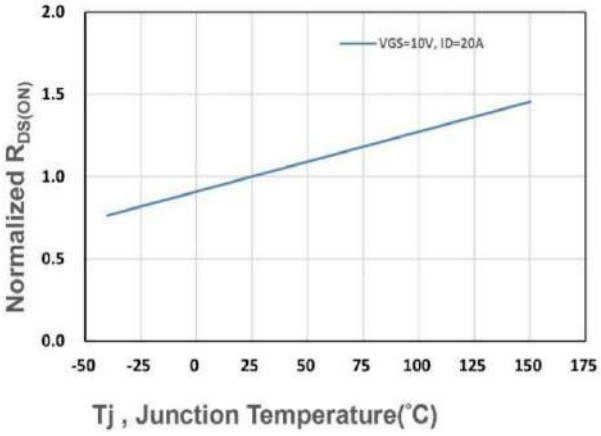


Figure 5.Normalized Threshold Voltage VS Junction Temparature

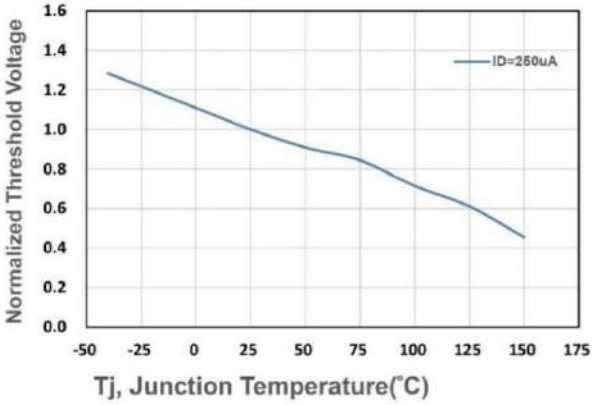


Figure 6. Typical Source-Drain Diode Forward Voltage

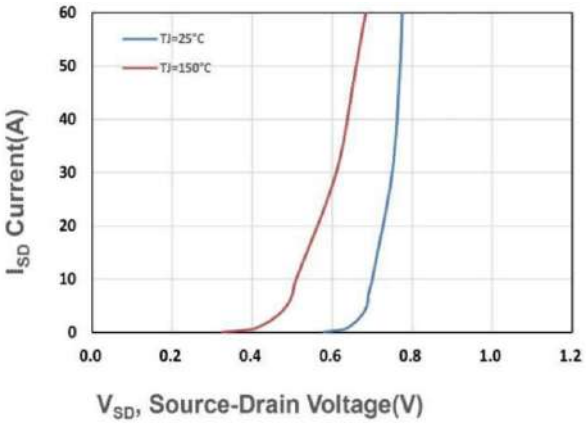


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

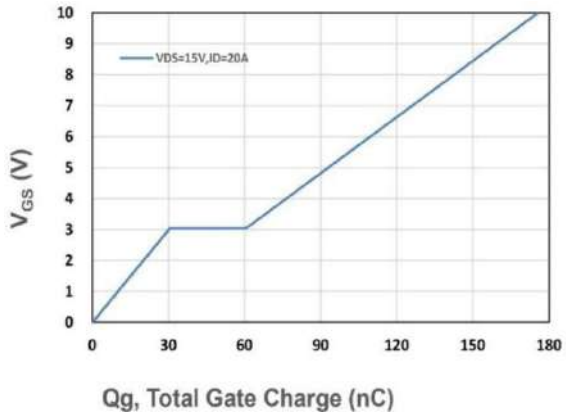


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

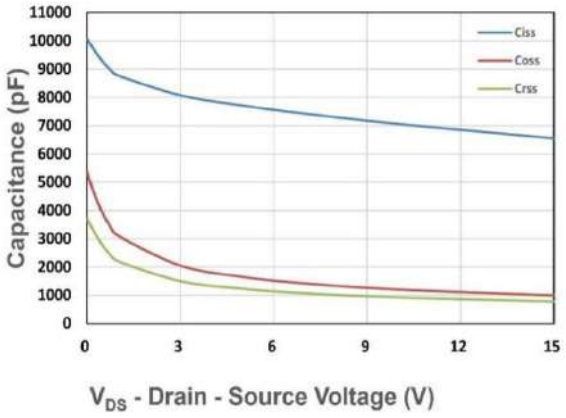


Figure 9. Maximum Safe Operating Area

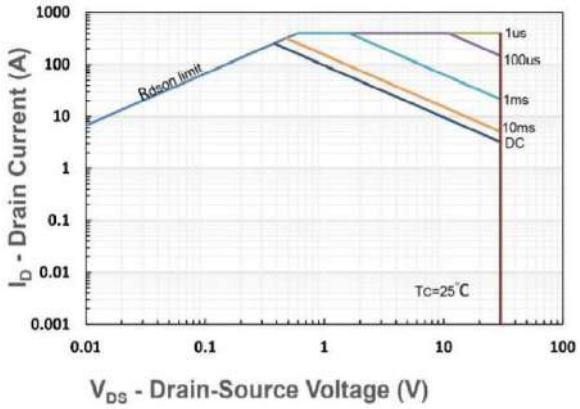


Figure 10. Maximun Drain Current vs. Case Temperature

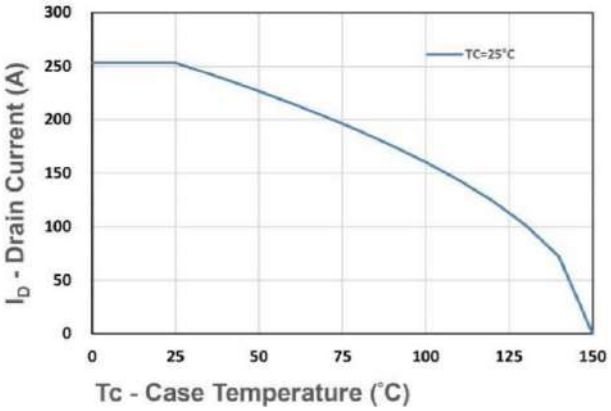
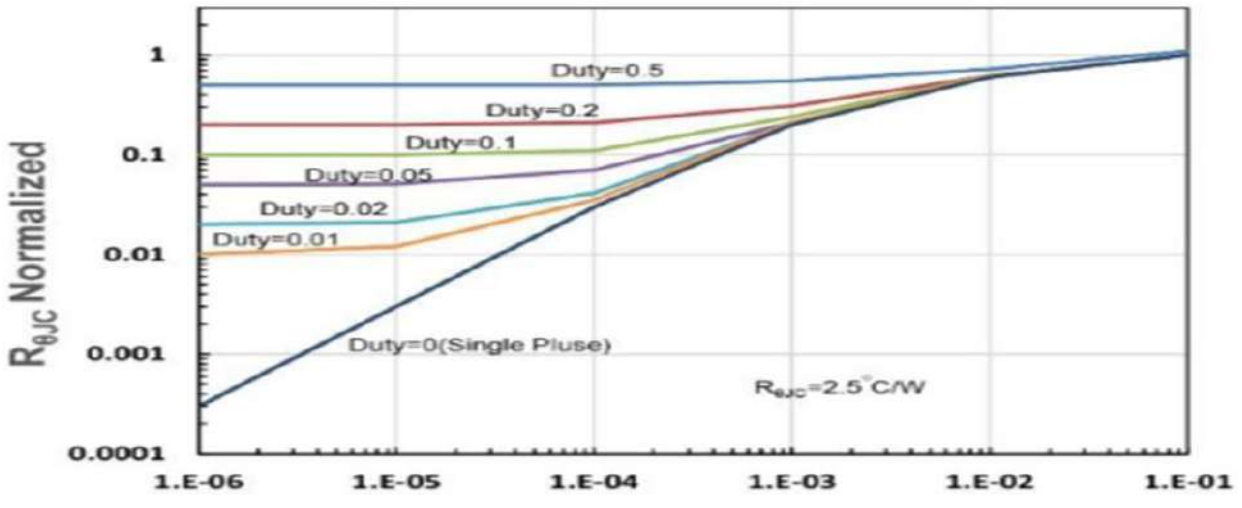
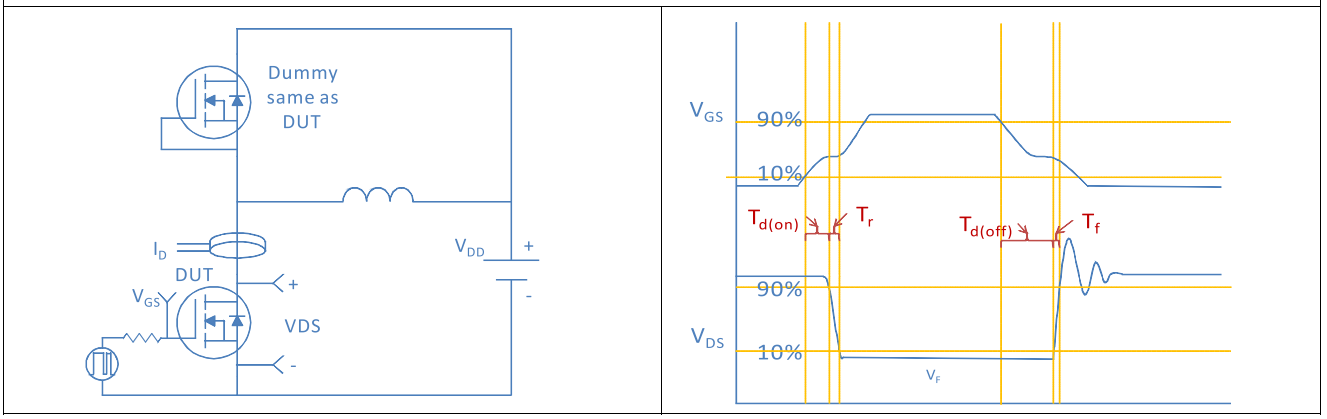


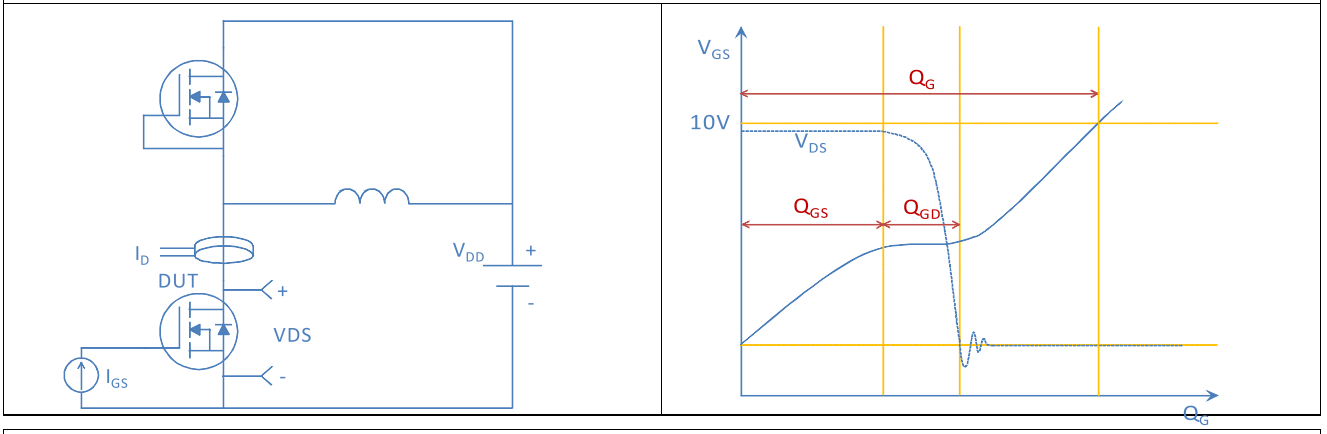
Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Case



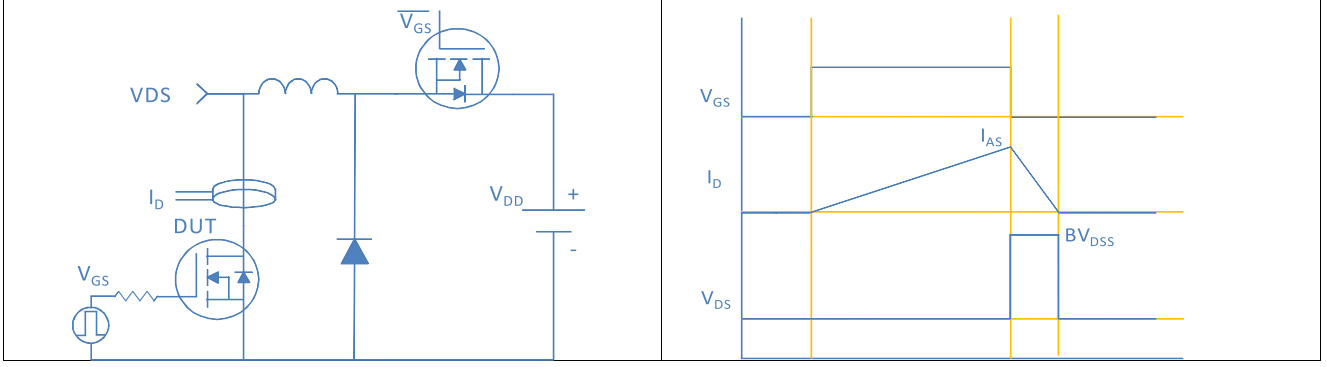
Inductive switching Test



Gate Charge Test



Uclamped Inductive Switching (UIS) Test



Diode Recovery Test