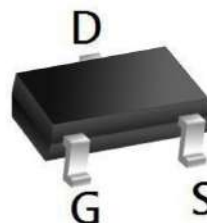


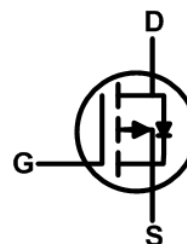
P-Ch 30V Fast Switching MOSFETs

Features:

- ★ 100% EAS Guaranteed
- ★ Green Device Available
- ★ Super Low Gate Charge
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology



SOT23 Pin Configuration



Description:

The KWN3103 is the high cell density trenched P-ch MOSFETs, which provide excellent $R_{DS(on)}$ and gate charge for most of the synchronous buck converter applications.

The KWN3103 meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

Product Summary

BVDSS	$R_{DS(on)}$	I_D
-30V	32mΩ	-4.8A

Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		10s	Steady State	
V_{DS}	Drain-Source Voltage	-30		V
V_{GS}	Gate-Source Voltage	± 20		V
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-5.5	-4.8	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ -10V^1$	-4.3	-3.8	A
I_{DM}	Pulsed Drain Current ²	-24		A
$P_D @ T_A = 25^\circ C$	Total Power Dissipation ³	1.32	1	W
$P_D @ T_A = 70^\circ C$	Total Power Dissipation ³	0.84	0.64	W
T_{STG}	Storage Temperature Range	-55 to 150		$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150		$^\circ C$

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	---	125	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹ ($t \leq 10s$)	---	95	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	80	$^\circ C/W$

Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250uA	-30	---	---	V
ΔBV _{DSS} /ΔT _J	BV _{DSS} Temperature Coefficient	Reference to 25°C, I _D =-1mA	---	-0.022	---	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =-10V, I _D =-4A	---	---	32	mΩ
		V _{GS} =-4.5V, I _D =-2A	---	---	45	
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =-250uA	-1.0	---	-2.5	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient		---	4.6	---	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =-24V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =-24V, V _{GS} =0V, T _J =55°C	---	---	5	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =-5V, I _D =-4A	---	15	---	S
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	13	---	Ω
Q _g	Total Gate Charge (-4.5V)	V _{DS} =-15V, V _{GS} =-4.5V, I _D =-4A	---	9.7	---	nC
Q _{gs}	Gate-Source Charge		---	2.5	---	
Q _{gd}	Gate-Drain Charge		---	3	---	
T _{d(on)}	Turn-On Delay Time	V _{DD} =-15V, V _{GS} =-10V, R _G =3.3Ω, I _D =-4A	---	16.4	---	ns
T _r	Rise Time		---	20.2	---	
T _{d(off)}	Turn-Off Delay Time		---	55	---	
T _f	Fall Time		---	10	---	
C _{iss}	Input Capacitance	V _{DS} =-15V, V _{GS} =0V, f=1MHz	---	942	---	pF
C _{oss}	Output Capacitance		---	165	---	
C _{rss}	Reverse Transfer Capacitance		---	137	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _S	Continuous Source Current ^{1,4}	V _G =V _D =0V, Force Current	---	---	-4.8	A
I _{SM}	Pulsed Source Current ^{2,4}		---	---	-24	A
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V, I _S =-1A, T _J =25°C	---	---	-1.2	V
t _{rr}	Reverse Recovery Time	I _F =-4A, dI/dt=100A/μs, T _J =25°C	---	18.3	---	nS
Q _{rr}	Reverse Recovery Charge		---	7.2	---	nC

Note :

1. The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.

2. The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%

3. The power dissipation is limited by 150°C junction temperature

4. The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

Typical Characteristics

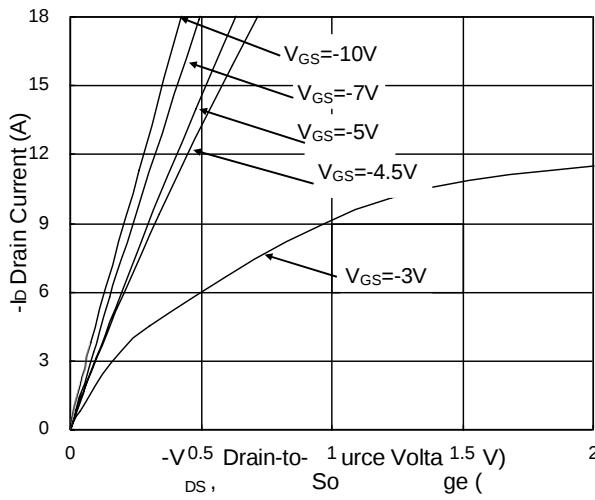


Fig.1 Typical Output Characteristics

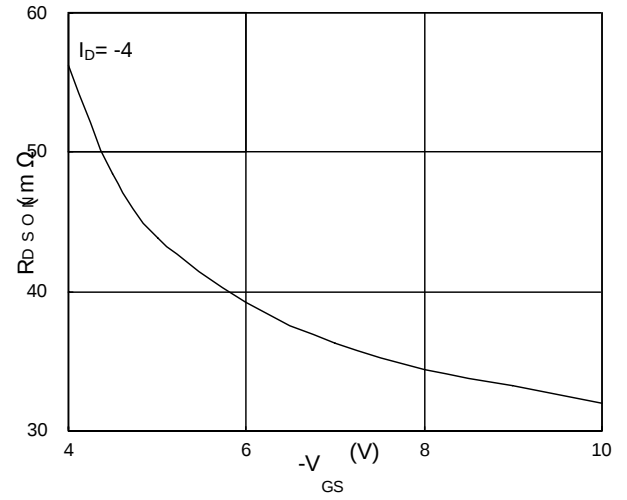


Fig.2 On-Resistance v.s Gate-Source

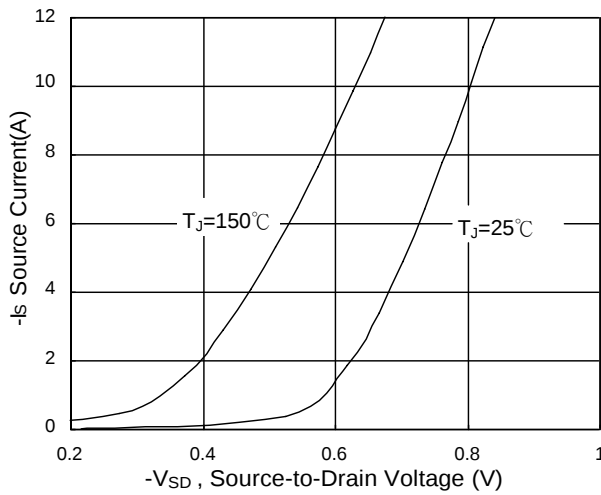


Fig.3 Forward Characteristics of Reverse

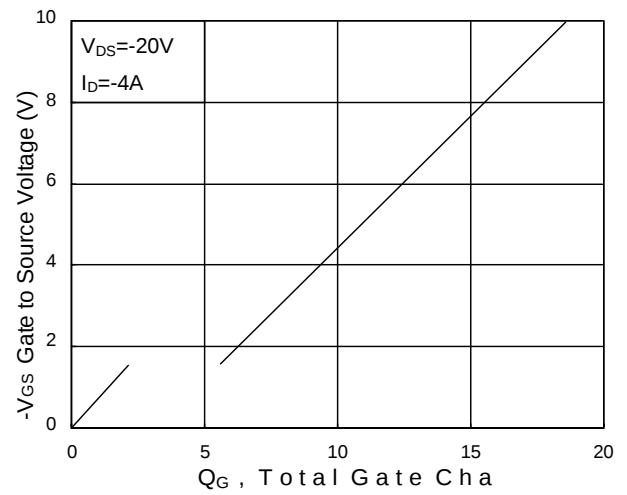


Fig.4 Gate-Charge Characteristics

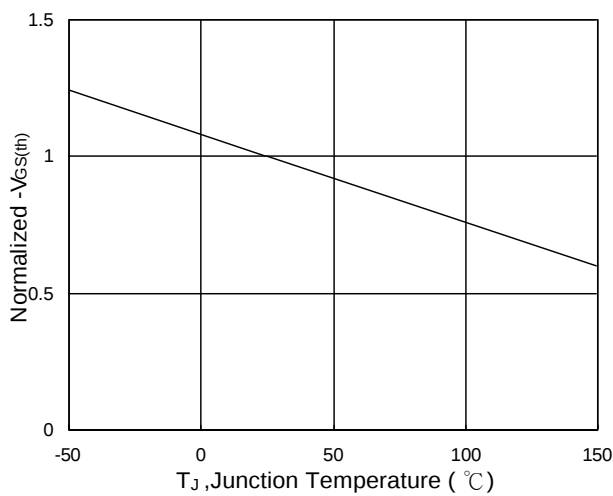


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

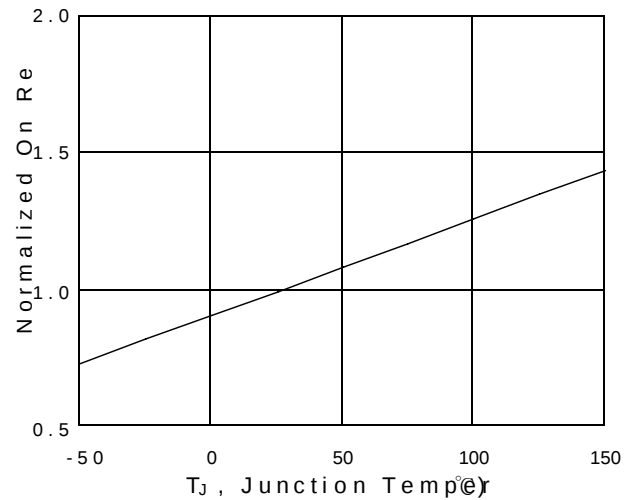


Fig.6 Normalized $R_{DS(on)}$ v.s T_J

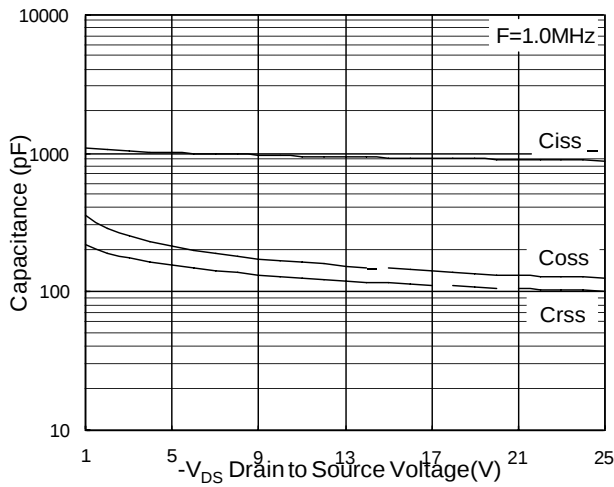


Fig.7 Capacitance

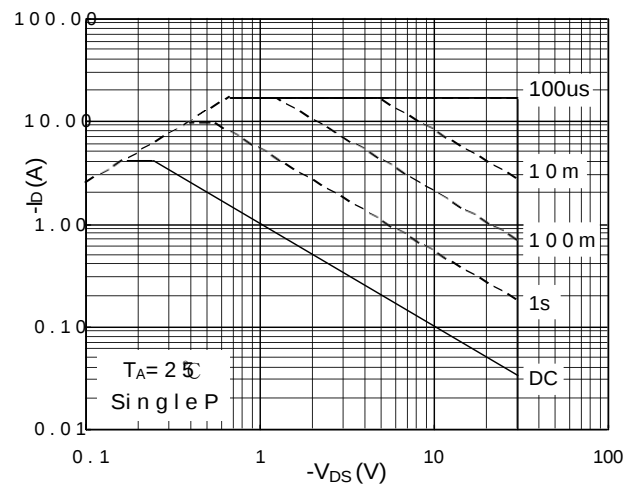


Fig.8 Safe Operating Area

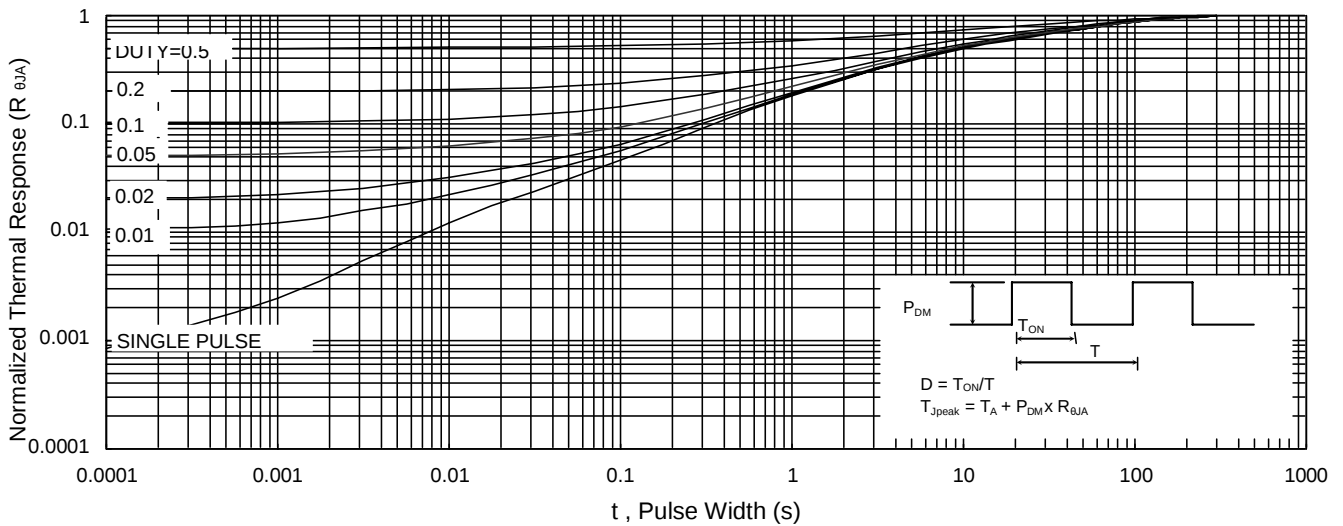


Fig.9 Normalized Maximum Transient Thermal Impedance

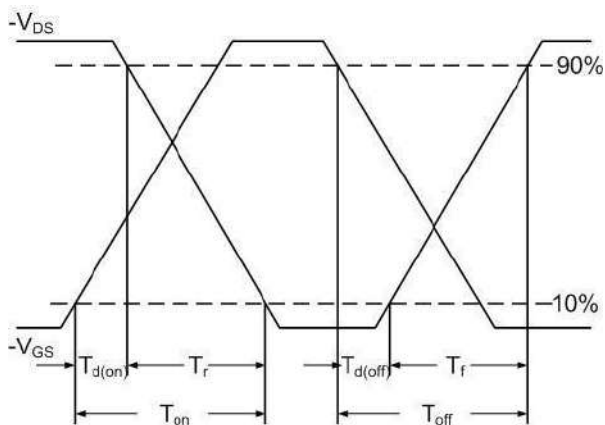


Fig.10 Switching Time Waveform

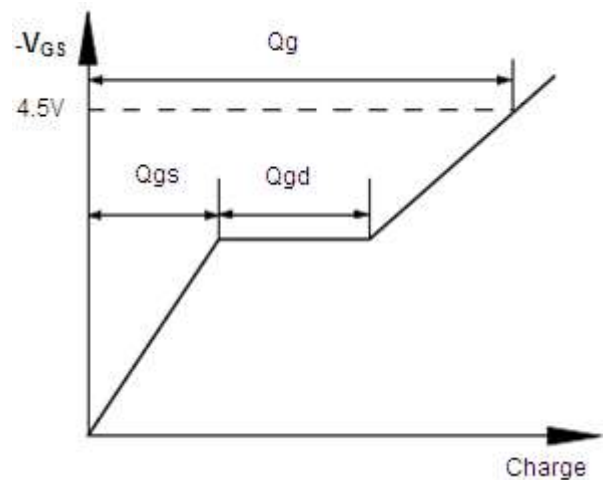


Fig.11 Gate Charge Waveform