

P-Ch 30V Fast Switching MOSFETs

Features:

- ★ 100% EAS Guaranteed
- ★ Green Device Available
- ★ Super Low Gate Charge
- ★ Excellent CdV/dt effect decline
- ★ Advanced high cell density Trench technology

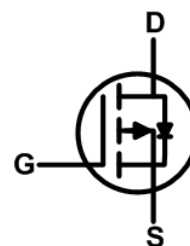


SOT223 Pin Configuration

Description:

The KWL3101 is the high cell density trenched P-ch MOSFETs, which provide excellent $R_{DS(on)}$ and gate charge for most of the synchronous buck converter applications.

The KWL3101 meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.



Product Summary

BVDSS	$R_{DS(on)}$	I_D
-30V	52m Ω	-4.5A

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-30	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_A=25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ -10V ¹	-4.5	A
$I_D@T_A=70^\circ\text{C}$	Continuous Drain Current, V_{GS} @ -10V ¹	-3.5	A
I_{DM}	Pulsed Drain Current ²	-23	A
$P_D@T_A=25^\circ\text{C}$	Total Power Dissipation ³	1.5	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	---	85	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	48	$^\circ\text{C/W}$

Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-30	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BV_{DSS} Temperature Coefficient	Reference to 25°C , $I_D=-1\text{mA}$	---	-0.023	---	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance ²	$V_{GS}=-10V, I_D=-4A$	---	42	52	$m\Omega$
		$V_{GS}=-4.5V, I_D=-3A$	---	75	90	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=-250\mu A$	-1.2	-1.6	-2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	4	---	$mV/^\circ\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=-24V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	-1	μA
		$V_{DS}=-24V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	-5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=-5V, I_D=-4A$	---	11	---	S
Q_g	Total Gate Charge (-4.5V)	$V_{DS}=-15V, V_{GS}=-4.5V, I_D=-4A$	---	6.4	9.0	nC
Q_{gs}	Gate-Source Charge		---	2.3	3.2	
Q_{gd}	Gate-Drain Charge		---	1.9	2.7	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=-15V, V_{GS}=-10V, R_G=3.3\Omega, I_D=-4A$	---	2.8	5.6	ns
T_r	Rise Time		---	8.4	15.1	
$T_{d(off)}$	Turn-Off Delay Time		---	39	78.0	
T_f	Fall Time		---	6	12.0	
C_{iss}	Input Capacitance	$V_{DS}=-15V, V_{GS}=0V, f=1\text{MHz}$	---	583	816	pF
C_{oss}	Output Capacitance		---	100	140	
C_{rss}	Reverse Transfer Capacitance		---	80	112	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,4}	$V_G=V_D=0V$, Force Current	---	---	-4.5	A
I_{SM}	Pulsed Source Current ^{2,4}		---	---	-23	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=-1A, T_J=25^\circ\text{C}$	---	---	-1.2	V
t_{rr}	Reverse Recovery Time	$I_F=-4A, dI/dt=100A/\mu s, T_J=25^\circ\text{C}$	---	7.8	---	nS
Q_{rr}	Reverse Recovery Charge		---	2.5	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3.The power dissipation is limited by 150°C junction temperature
- 4.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

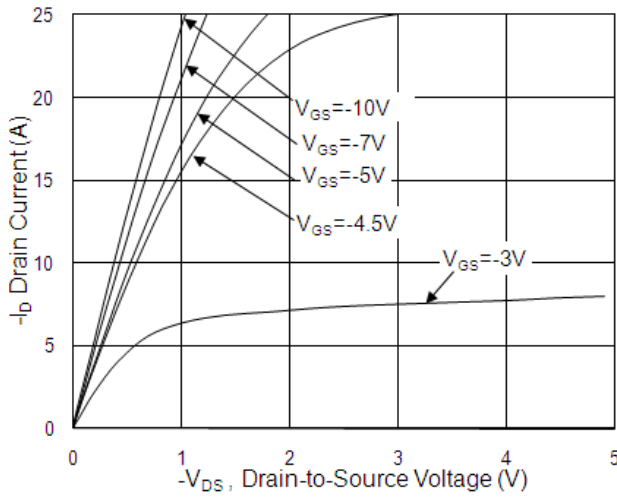


Fig.1 Typical Output Characteristics

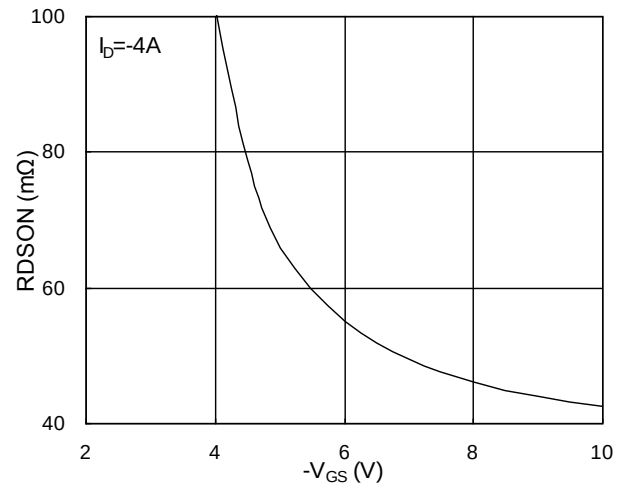


Fig.2 On-Resistance v.s Gate-Source

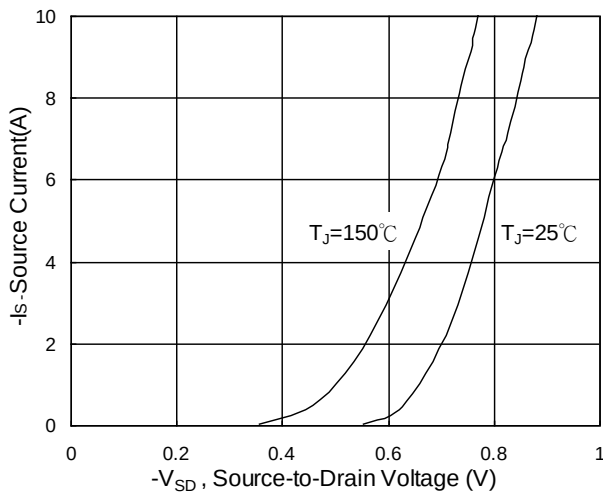


Fig.3 Forward Characteristics Of Reverse

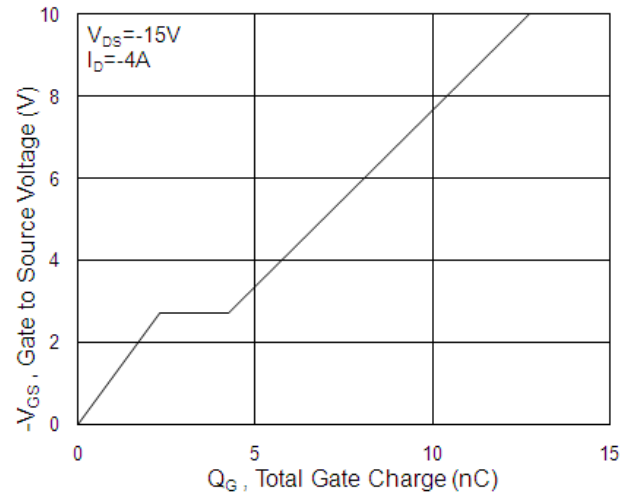


Fig.4 Gate Charge Characteristics

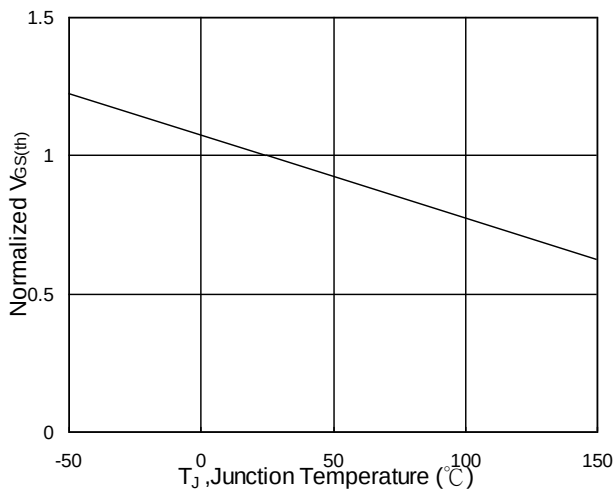


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

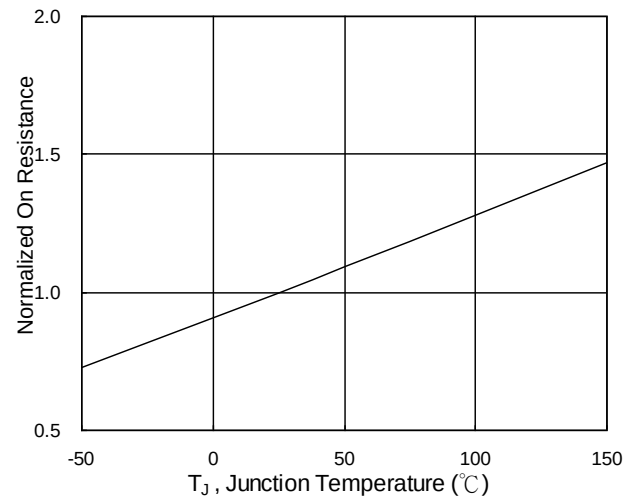


Fig.6 Normalized $R_{DS(on)}$ v.s T_J

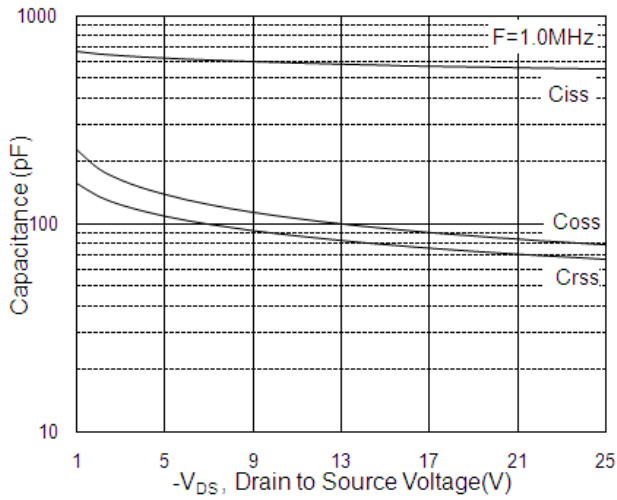


Fig.7 Capacitance

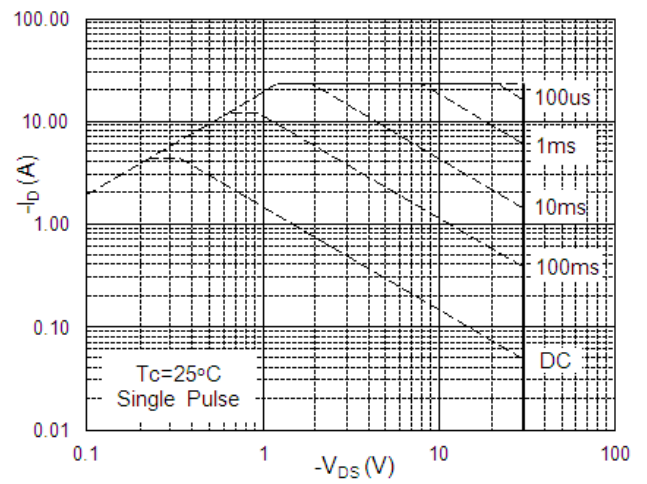


Fig.8 Safe Operating Area

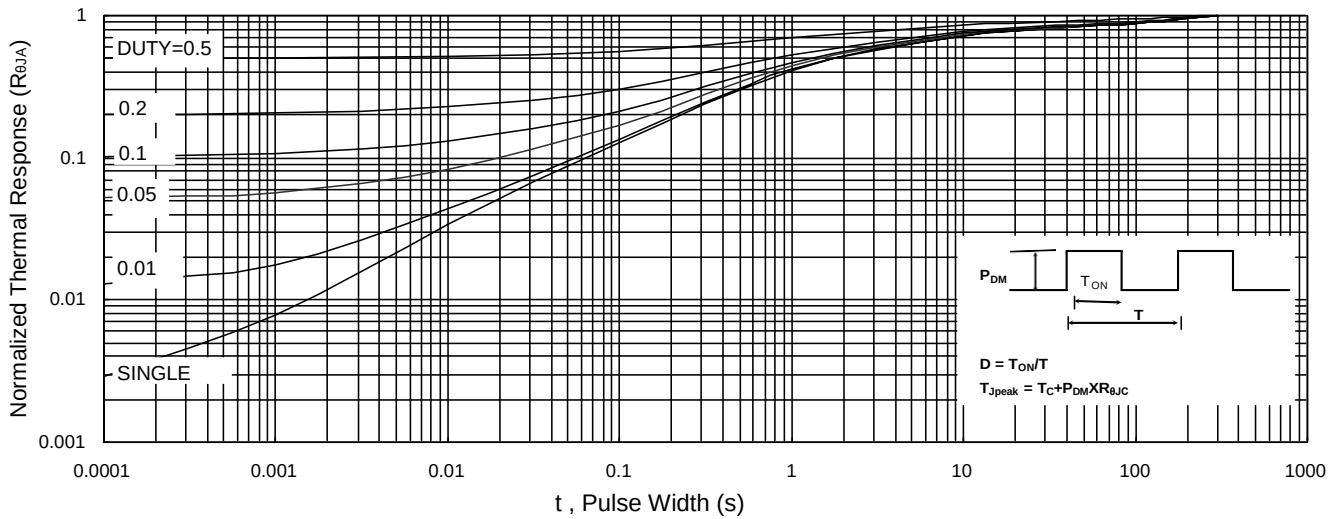


Fig.9 Normalized Maximum Transient Thermal Impedance

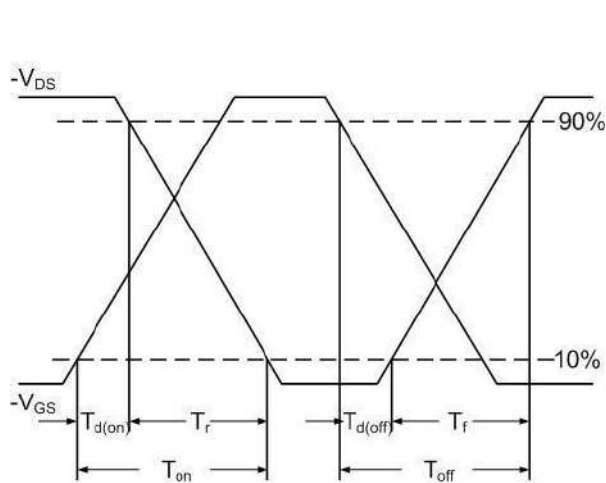


Fig.10 Switching Time Waveform

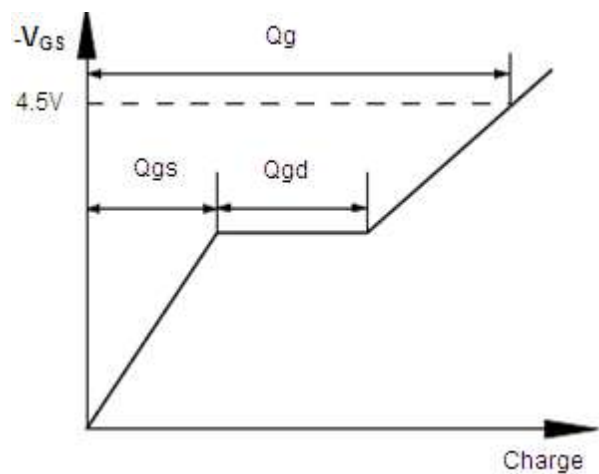


Fig.11 Gate Charge Waveform