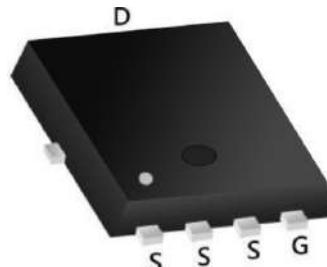


N-Ch 40V Fast Switching MOSFETs

Features:

- ★ 100% UIS Tested
- ★ Advanced Trench Technology
- ★ Low Gate Charge
- ★ High Current Capability
- ★ RoHS and Halogen-Free Compliant



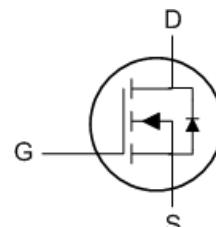
Applications:

- SMPS Synchronous Rectification
- DC/DC Converters
- Or-ing

Product Summary

BVDSS	RDS(on)	ID
40V	1.8mΩ	100A

PRPAK5X6 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	40	V
V _{GS}	Gate-Source Voltage	±20	V
I _D @T _c =25°C	Continuous Drain Current, V _{GS} @ 10V ^{1,6}	100	A
I _D @T _c =100°C	Continuous Drain Current, V _{GS} @ 10V ^{1,6}	82	A
I _{DM}	Pulsed Drain Current ²	400	A
EAS	Single Pulse Avalanche Energy ³	400	mJ
I _{AS}	Avalanche Current	40	A
P _D @T _c =25°C	Total Power Dissipation ⁴	83	W
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R _{θJA}	Thermal Resistance Junction-Ambient ¹	---	50	°C/W
R _{θJC}	Thermal Resistance Junction-Case ¹	---	1.5	°C/W

Electrical Characteristics ($T_J=25^{\circ}\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}$, $I_D=250\mu\text{A}$	40	---	---	V
$R_{\text{DS(ON)}}$	Static Drain-Source On-Resistance ²	$V_{\text{GS}}=10\text{V}$, $I_D=20\text{A}$	---	1.5	1.8	$\text{m}\Omega$
		$V_{\text{GS}}=4.5\text{V}$, $I_D=20\text{A}$	---	2.0	2.6	
$V_{\text{GS(th)}}$	Gate Threshold Voltage	$V_{\text{GS}}=V_{\text{DS}}$, $I_D=250\mu\text{A}$	1.2	1.6	2.2	V
I_{DSS}	Drain-Source Leakage Current	$V_{\text{DS}}=32\text{V}$, $V_{\text{GS}}=0\text{V}$, $T_J=25^{\circ}\text{C}$	---	---	1	uA
		$V_{\text{DS}}=32\text{V}$, $V_{\text{GS}}=0\text{V}$, $T_J=55^{\circ}\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{\text{GS}}=\pm 20\text{V}$, $V_{\text{DS}}=0\text{V}$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{\text{DS}}=5\text{V}$, $I_D=20\text{A}$	---	53	---	S
R_g	Gate Resistance	$V_{\text{DS}}=0\text{V}$, $V_{\text{GS}}=0\text{V}$, $f=1\text{MHz}$	---	1.0	---	Ω
Q_g	Total Gate Charge (4.5V)	$V_{\text{DS}}=15\text{V}$, $V_{\text{GS}}=10\text{V}$, $I_D=20\text{A}$	---	45	---	nC
Q_{gs}	Gate-Source Charge		---	12	---	
Q_{gd}	Gate-Drain Charge		---	18.5	---	
$T_{\text{d(on)}}$	Turn-On Delay Time	$V_{\text{DD}}=15\text{V}$, $V_{\text{GS}}=10\text{V}$, $R_G=3.3\Omega$, $I_D=20\text{A}$	---	18.5	---	ns
T_r	Rise Time		---	9	---	
$T_{\text{d(off)}}$	Turn-Off Delay Time		---	58.5	---	
T_f	Fall Time		---	32	---	
C_{iss}	Input Capacitance	$V_{\text{DS}}=20\text{V}$, $V_{\text{GS}}=0\text{V}$, $f=1\text{MHz}$	---	3972	---	pF
C_{oss}	Output Capacitance		---	1119	---	
C_{rss}	Reverse Transfer Capacitance		---	82	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_s	Continuous Source Current ^{1,6}	$V_G=V_D=0\text{V}$, Force Current	---	---	100	A
V_{SD}	Diode Forward Voltage ²	$V_{\text{GS}}=0\text{V}$, $I_s=1\text{A}$, $T_J=25^{\circ}\text{C}$	---	---	1.2	V

Note :

1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
2. The data tested by pulsed , pulse width $\leq 300\text{us}$, duty cycle $\leq 2\%$
3. The EAS data shows Max. rating . The test condition is $V_{\text{DD}}=25\text{V}$, $V_{\text{GS}}=10\text{V}$, $L=0.5\text{mH}$, $I_{\text{AS}}=40\text{A}$
4. The power dissipation is limited by 150°C junction temperature
5. The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.
6. Package limitation current is 100A.

Typical Characteristics

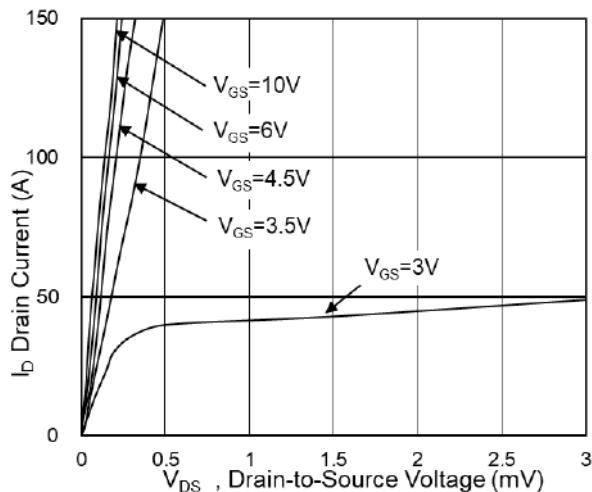


Fig.1 Typical Output Characteristics

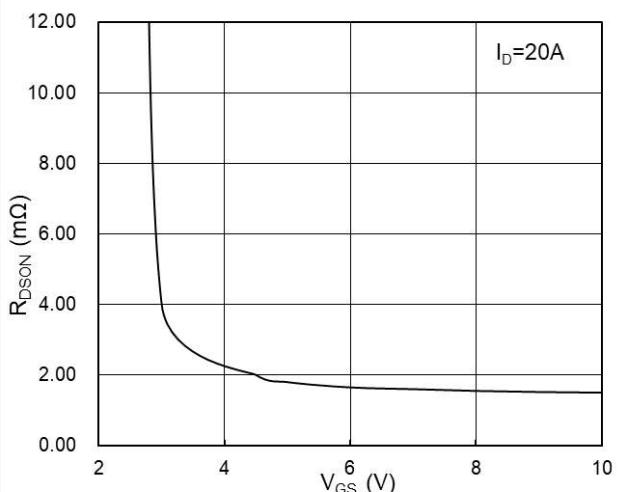


Fig.2 On-Resistance vs G-S Voltage

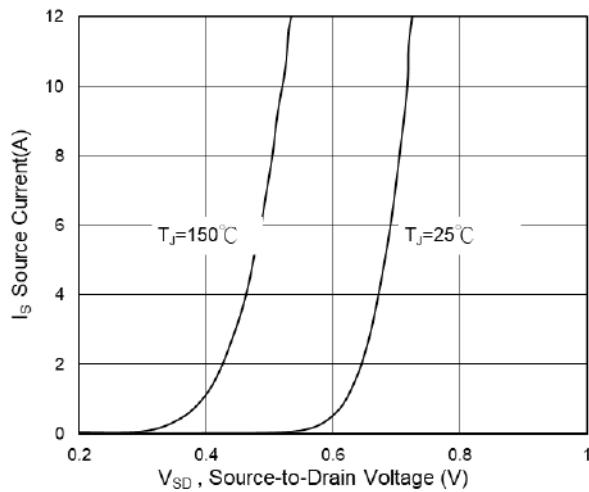


Fig.3 Source Drain Forward Characteristics

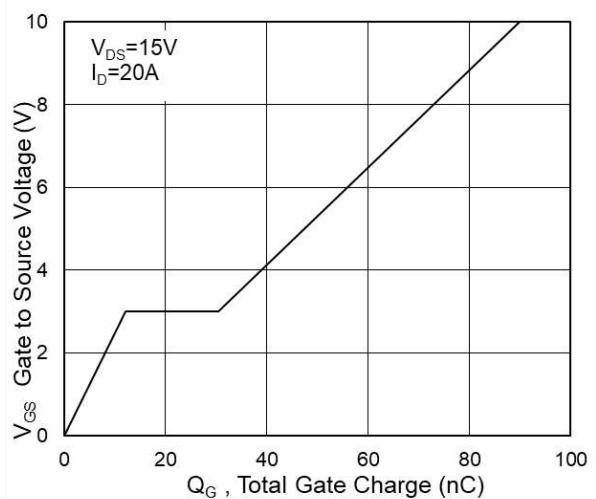


Fig.4 Gate-Charge Characteristics

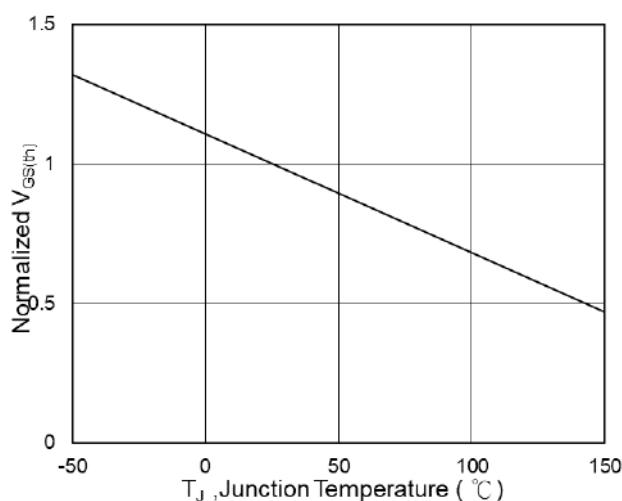


Fig.5 Normalized $V_{GS(th)}$ vs T_J

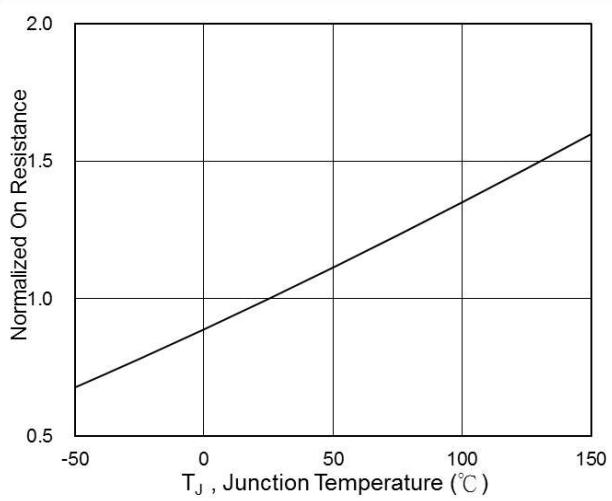


Fig.6 Normalized $R_{DS(on)}$ vs T_J

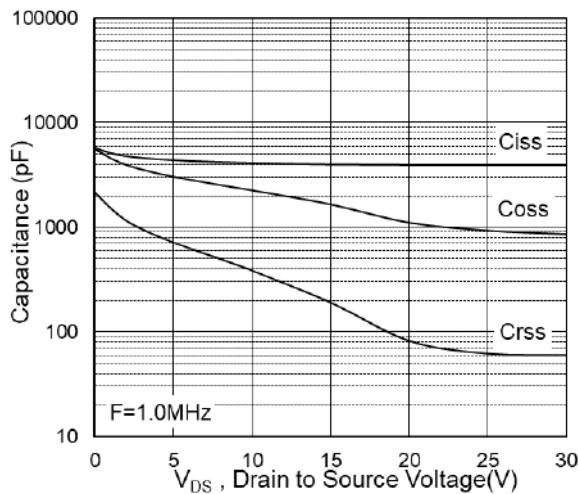


Fig.7 Capacitance

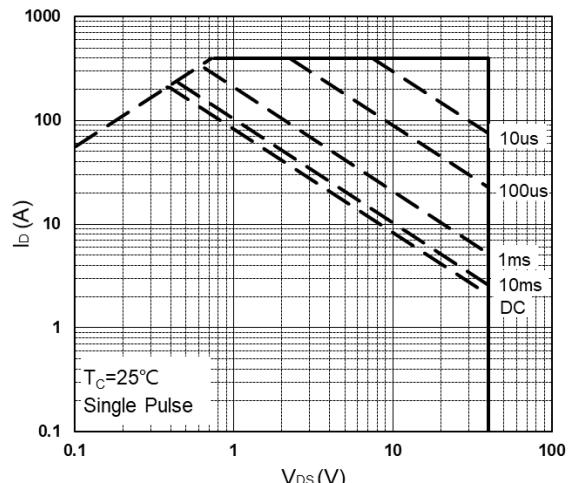


Fig.8 Safe Operating Area

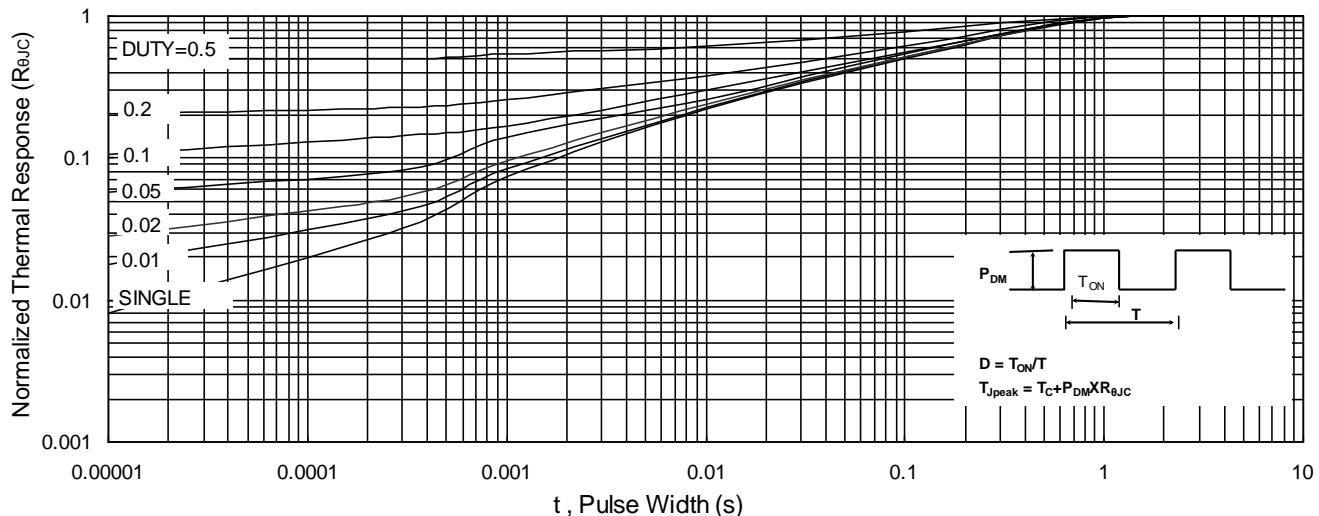


Fig.9 Normalized Maximum Transient Thermal Impedance

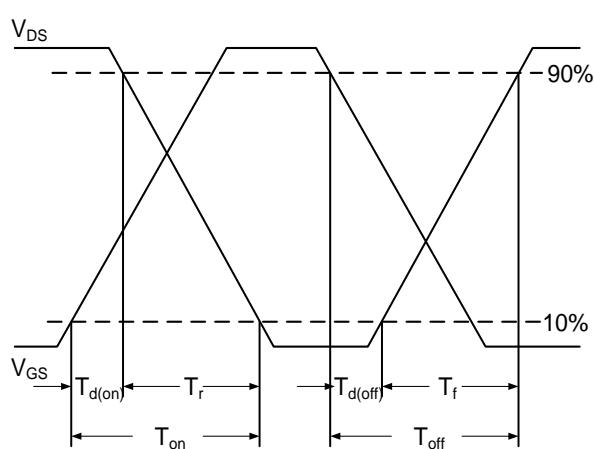


Fig.10 Switching Time Waveform

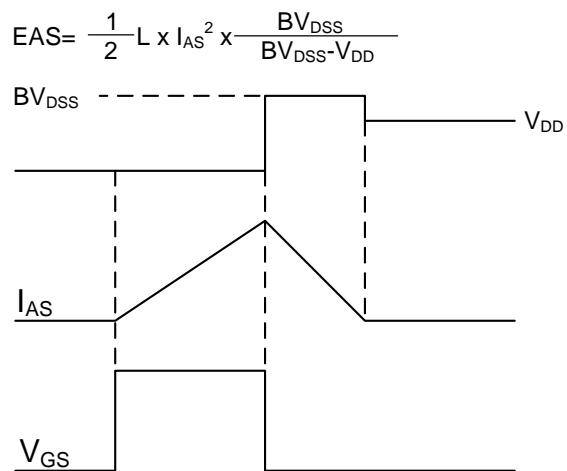


Fig.11 Unclamped Inductive Switching Waveform