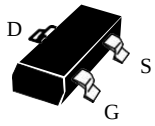
N-Channel High Density Trench MOSFET

Features:

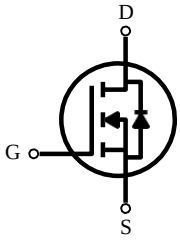
SOT-23-3L



- Super high dense cell trench design for low $R_{DS(on)}$.
- Rugged and reliable.
- Surface Mount package.

PRODUCT SUMMARY

V_{DSS}	I_D	$R_{DS(on)}$ (mΩ) Max
100V	1.2A	310@ V_{GS} = 10V
	0.7A	330@ V_{GS} = 4.5V



ABSOLUTE MAXIMUM RATINGS (T_A = 25 ℃ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	± 20	V
Drain Current-Continuous[a] @ T_A = 25 ℃		I_D	1.2	A
-Pulse [b]		I_{DM}	5	A
Drain-Source Diode Forward Current [a]		I_S	1	A
Maximum Power Dissipation [a]	T_A=25℃	P_D	1	W
	T_A=75℃		0.6	
1. Operating Junction and Storage Temperature Range		T_J,T_{STG}	- 55 to 150	℃

THERMAL CHARACTERISTICS

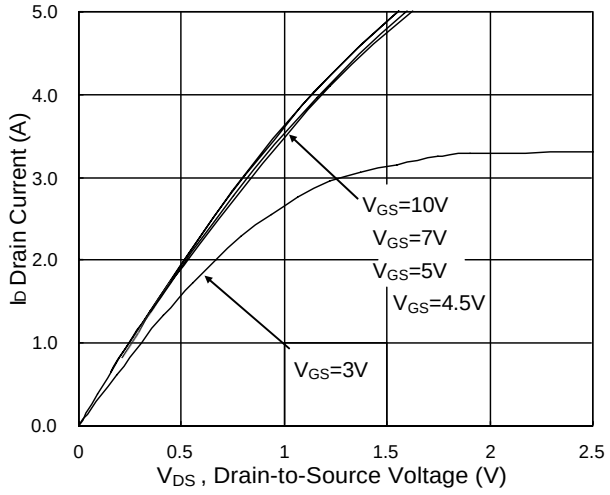
Thermal Resistance,Junction-to-Ambient[a]	R_{thJA}	125	℃/W

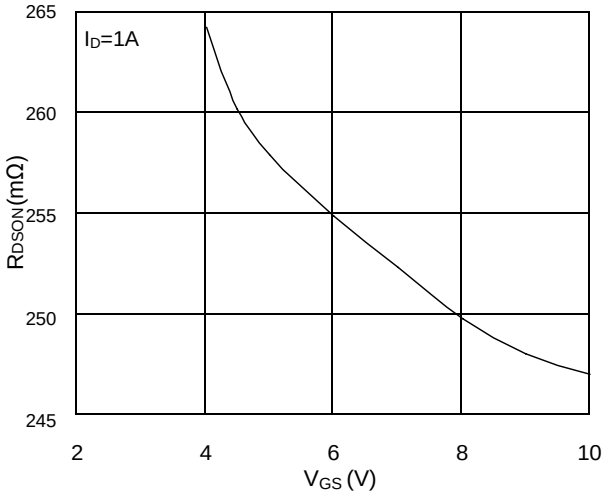
Note：
a. Surface Mounted on FR4 Board , t ≤ 10sec .
b. Pulse width limited by maximum junction temperature.

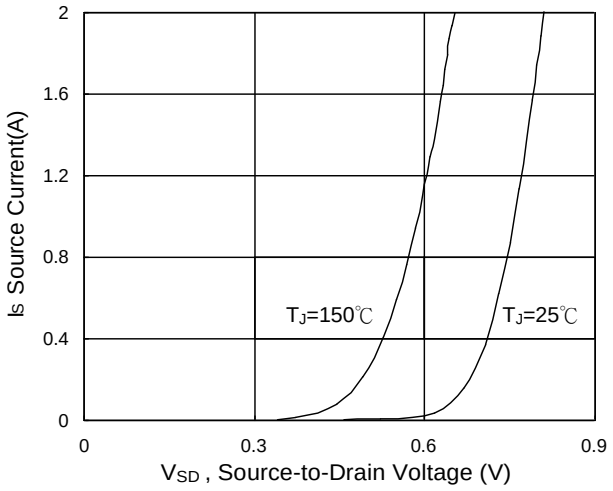
ELECTRICAL CHARACTERISTICS (T_A = 25 ℃ unless otherwise noted)

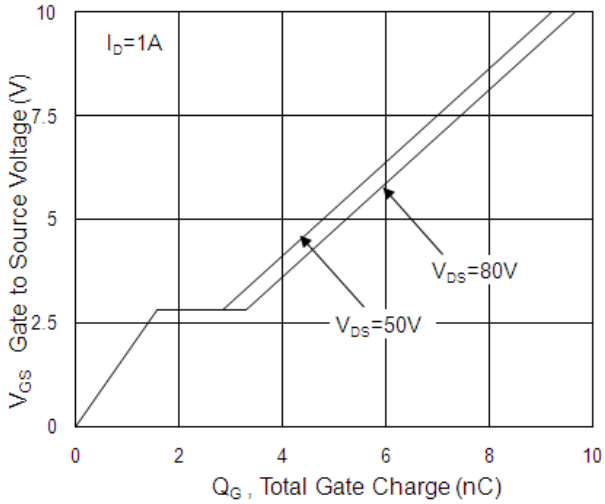
Parameter	Symbol	Condition	Min	Typ[c]	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V , I_D = 250uA	100			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 80V , V_{GS} = 0V			1	uA
Gate-Body Leakage	I_{GSS}	V_{GS} = ±20V , V_{DS} = 0V			±100	nA
ON CHARACTERISTICS[b]						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS} , I_D = 250uA	1	1.5	2.5	V
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10V , I_D = 1.2A		260	310	mΩ
		V_{GS} = 4.5V , I_D = 0.7A		280	330	
Forward Transconductance	g_{fs}	V_{DS} = 5V , I_D = 1.2A		2.4		S
DRAIN-SOURCE DIODE CHARACTERISTICS[b]						
Diode Forward Voltage	V_{SD}	V_{GS} = 0V , I_S = 1.0A			1.2	V
DYNAMIC CHARACTERISTICS[c]						
Input Capacitance	C_{ISS}	V_{DS} = 15V , V_{GS} = 0V f = 1.0MHz		508		pF
Output Capacitance	C_{OSS}			29		pF
Reverse Transfer Capacitance	C_{RSS}			16.4		pF
SWITCHING CHARACTERISTICS[c]						
Turn-On Delay Time	$t_{D(ON)}$	V_{DD} = 50V , I_D = 1A V_{GEN} = 10V R_L = 15 Ω R_{GEN} = 6 Ω		1.6		ns
Rise Time	t_r			19		ns
Turn-Off Delay Time	$t_{D(OFF)}$			13.6		ns
Fall Time	t_f			19		ns
Total Gate Charge	Q_g	V_{DS} = 80V I_D = 1A V_{GS} = 10V		9.7		nC
Gate-Source Charge	Q_{gs}			1.6		nC
Gate-Drain Charge	Q_{gd}			1.7		nC

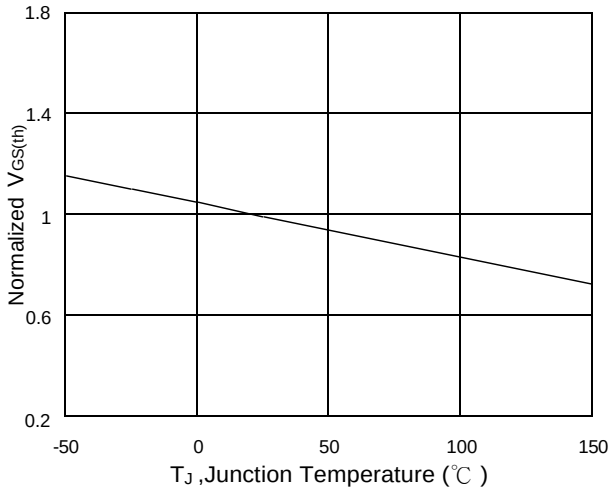
Note：
b. Pulse Test：Pulse width ≤ 300us , Duty Cycle ≤ 2% .
c. Guaranteed by design , not subject to production testing.

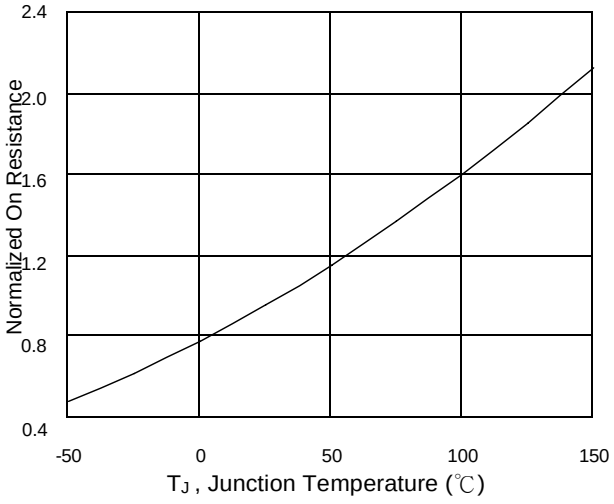

5.0
4.0
3.0
2.0
1.0
0.0
ID Drain Current (A)
VGS=10V
VGS=7V
VGS=5V
VGS=4.5V
VGS=3V
0
0.5
1
1.5
2
2.5
VDS , Drain-to-Source Voltage (V)

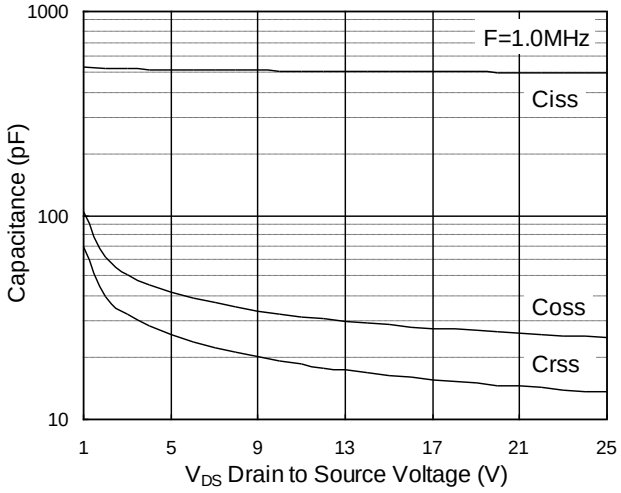

ID=1A
265
260
255
250
245
RDSON(mΩ)
2
4
6
8
10
VGS (V)

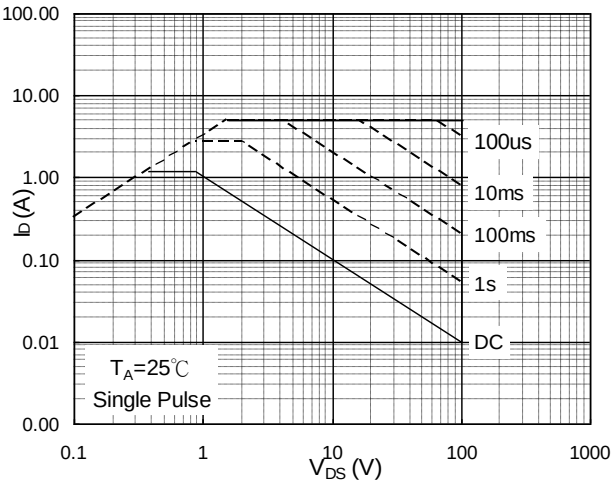

2
1.6
1.2
0.8
0.4
0
Is Source Current(A)
TJ=150℃
TJ=25℃
0
0.3
0.6
0.9
VSD , Source-to-Drain Voltage (V)

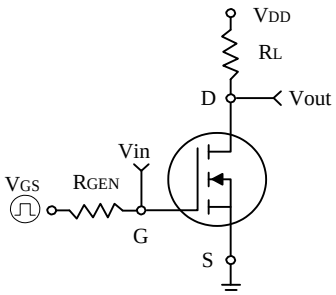

10
7.5
5
2.5
0
VGS Gate to Source Voltage (V)
ID=1A
VDS=80V
VDS=50V
0
2
4
6
8
10
QG , Total Gate Charge (nC)

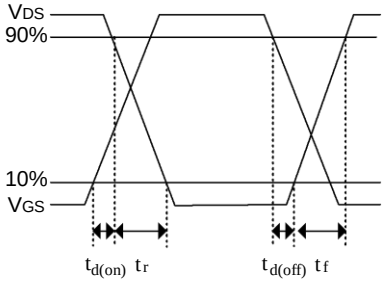

1.8
1.4
1
0.6
0.2
Normalized VGS(th)
-50
0
50
100
150
TJ ,Junction Temperature (℃)


2.4
2.0
1.6
1.2
0.8
0.4
Normalized On Resistance
-50
0
50
100
150
TJ , Junction Temperature (℃)

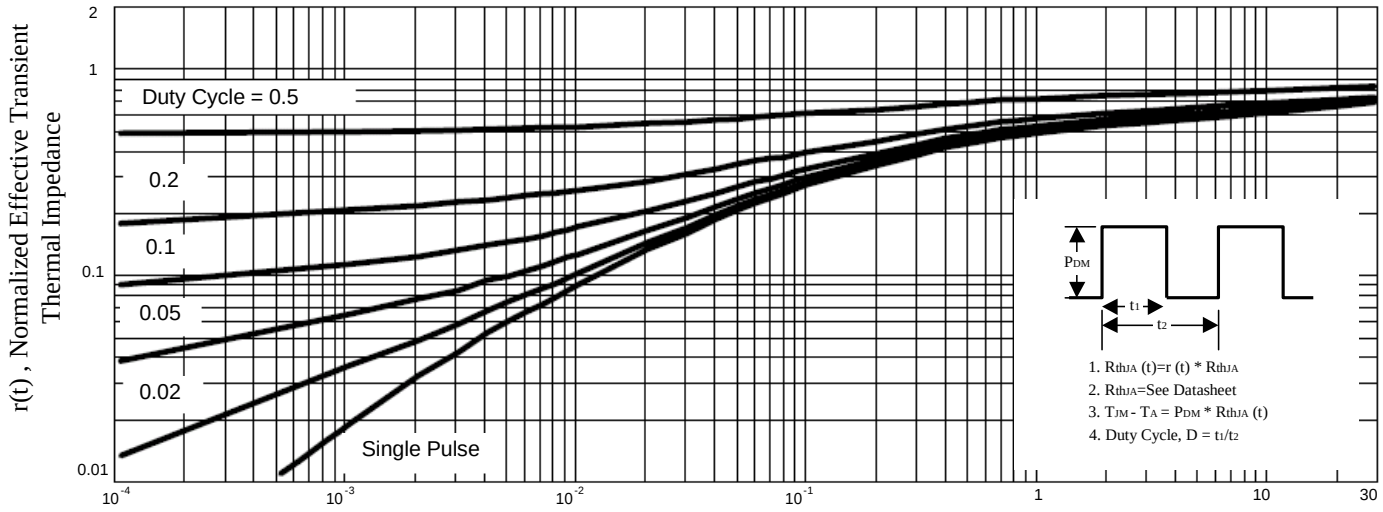








Switching Test Circuit and Switching Waveforms



Square Wave Pulse Duration (sec)

Normalized Thermal Transient Impedance Curve