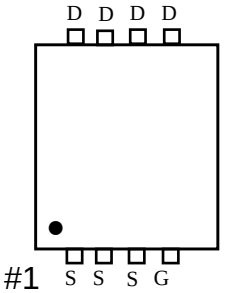
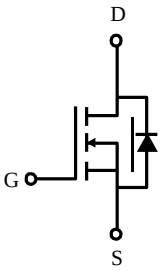
N-Channel High Density Trench MOSFET

Features:

- Super high dense cell trench design for low $R_{DS(on)}$.
- Rugged and reliable.
- Surface Mount package.

PDFN5x6





PRODUCT SUMMARY

$V_{(BR)DSS}$	$R_{DS(ON)}$	I_D
100V	8mΩ	78A

MARKING：0066

ABSOLUTE MAXIMUM RATINGS (T_A = 25 ℃ unless otherwise noted)

PARAME TERS TEST CONDITIONS		SYMBOL	LIMITS	UNITS
Gata-Source voltage		V_{GS}	±20	V
Continuous Drain current	T_C = 25℃	I_D	78	A
	T_C = 100 ℃		62	
Puised Drain Current[1]		I_{DM}	280	
Avalanche Current		I_{AS}	28	
Avalanche Energy	L=0.1mH	E_{AS}	39.2	mJ
Power Dissipation	T_C = 25 ℃	P_D	108	W
	T_C = 100 ℃		67	
Operaing junction & Storege Temperature Range		T_s,T_{stg}	-55 to 150	℃

THERMAL CHARACTERISTICS

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNITS
Junction-to-Case	$R_{\theta Jc}$		1.3	℃/W
Junction-to-Ambient	$R_{\theta JA}$		55	℃/W

ELECTRICAL CHARACTERISTICS (T_A = 25 ℃ unless otherwise noted)

PARAMETER	SYNBOL	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
STATIC						
Drain-Source Breakdown Voltege	$V_{(BR)DSS}$	V_{GS}=0V,I_D=250μA	100			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	2	3	4	V
Gate-Body Leakage	I_{GSS}	V_{DS}=0V,V_{GS}=± 20V			±100	nA
Zero Gate Voltage Dain Current	I_{DSS}	V_{DS}=80V,V_{GS}=0 V			1	μA
		V_{DS}=80V,V_{GS}=0V,T_J=125 ℃			30	μA
Drain-Source On- State Resistance[1]	$R_{DS(ON)}$	V_{GS}=10V,I_D=13.5A		6.6	8	mΩ
Forward Trans conductance[1]	g_{fs}	V_{DS}=10V,I_D=20A		80		S
DYNAMIC						
Input Capacitance	C_{iss}	V_{GS}=0V,V_{DS}=50V,f=1MHz		3148		pF
Output Capacitance	C_{oss}			693		pF
Reverse Transfer Capacitance	C_{rss}			26		pF
Gate Resistance	R_G	V_{GS}=0V,f=1MHz		3		Ω
Total Gate Charge[2]	$Q_{g(vgs=10V)}$	V_{DS}=50V (BR)DSS, I_D = 13.5A		45		nC
	$Q_{g(vgs=4.5V)}$			19.3		nC
Gate Source Charge[2]	$Q_{gS(VGS=10V)}$			9.5		nC
	$Q_{gS(VGS=4.5V)}$			6.5		nC
Gate-Drain Charge[2]	$Q_{gd(VGS=10V)}$			4.8		nC
	$Q_{gd(VGS=4.5V)}$			2.7		nC
Tum-On Delay Time[2]	$t_{d(on)}$	V_{DS}=50V,R_L=1.5Ω I_D =13.5A,V_{GS}=10V.R_{GS}=3Ω		10		nS
Rise Time[2]	t_r			6.5		nS
Tum-Off Delay Time[2]	$t_{d(off)}$			45		nS
Fall Time[2]	t_r			7.5		nS
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS(T_J=25℃)						
Continuous Current	I_S			45		A
Forward Voltage[1]	V_{SD}	I_F=I_S,V_{GS}=0V		0.75	1.1	V
Reverse Recovery Time	T_{rr}	I_F=13.5A,d_{1f}/d_t=100A/μs		33		nS
Reverse Recovery Charge	Q_{rr}			150		nC

Note
b. Pulse Test Pulse width ≤ 300usec , Duty Cycle ≤ 2% .
c. Independent of operating production testing .

Typical Characteristics

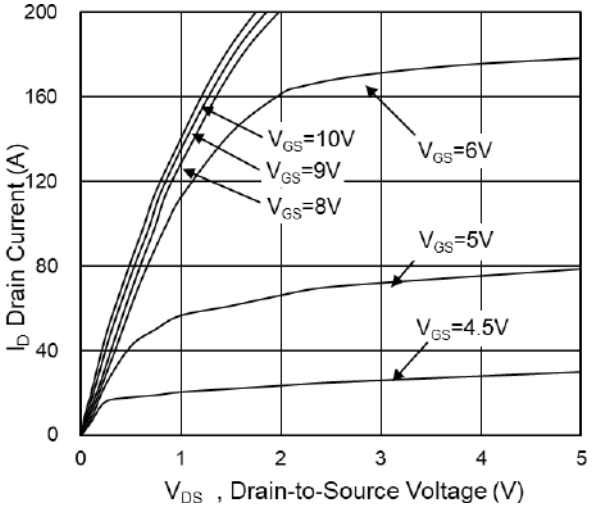


Fig.1 Typical Output Characteristics

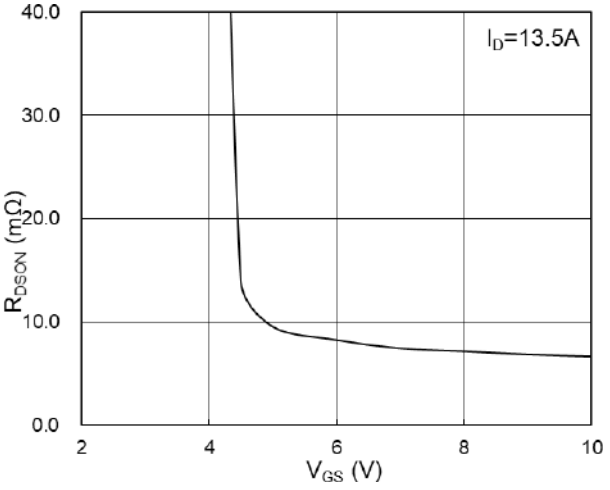


Fig.2 On-Resistance vs G-S Voltage

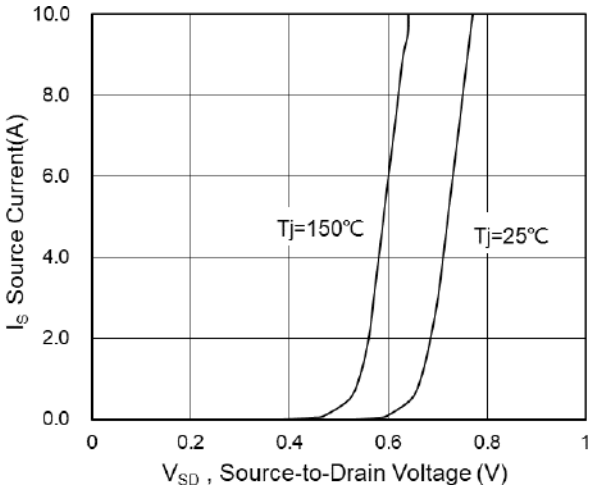


Fig.3 Source-Drain Forward Characteristics

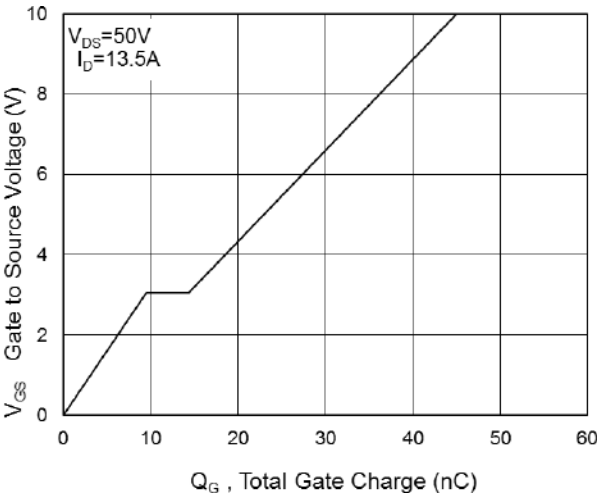


Fig.4 Gate-Charge Characteristics

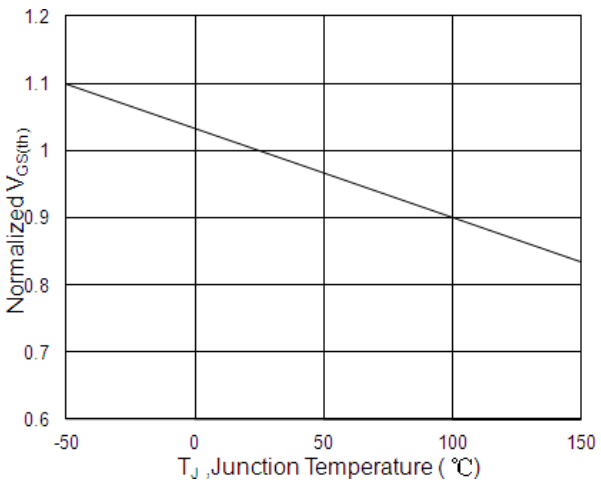


Fig.5 Normalized $V_{GS(th)}$ vs T_J

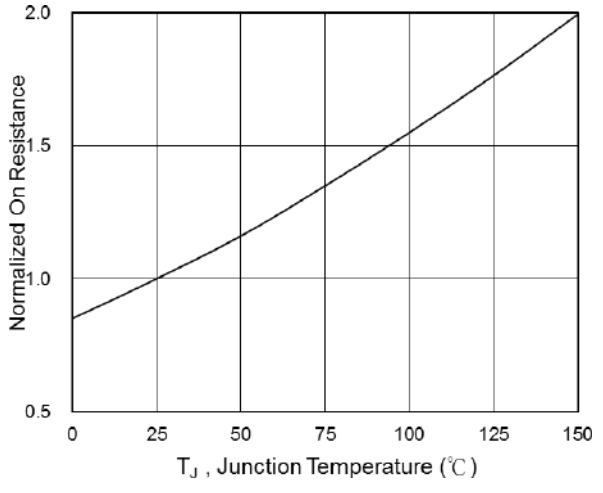


Fig.6 Normalized R_{DSON} vs T_J

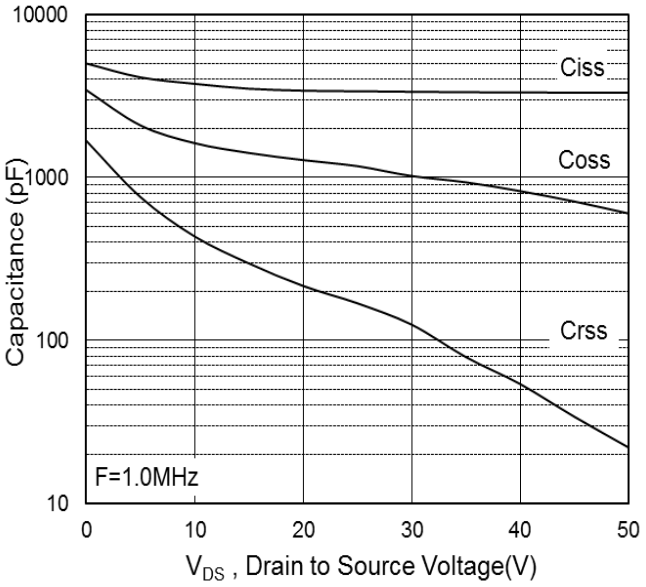


Fig.7 Capacitance

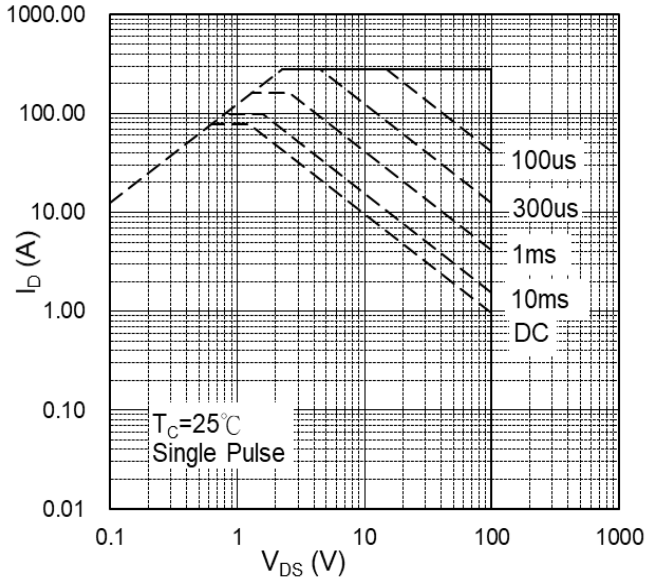


Fig.8 Safe Operating Area

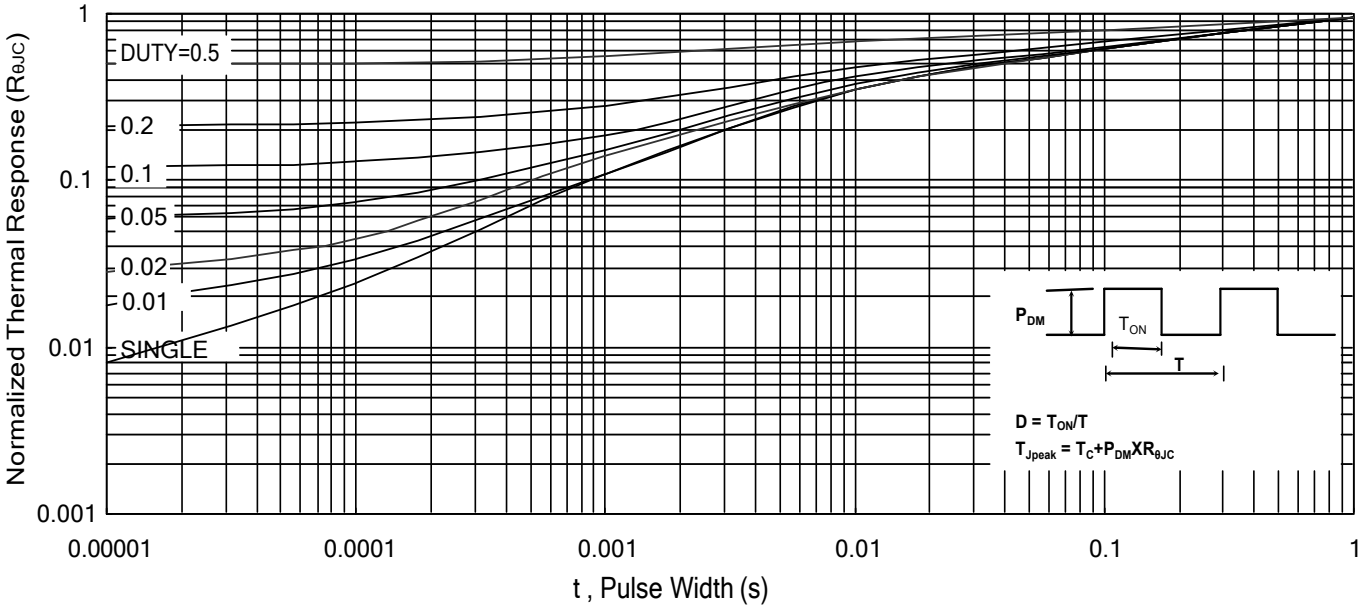


Fig.9 Normalized Maximum Transient Thermal Impedance