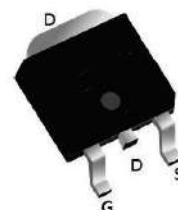


N-Channel High Density Trench MOSFET

Features:

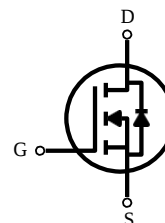
- Super high dense cell trench design for low $R_{DS(on)}$.
- Rugged and reliable.
- Surface Mount package.

TO - 252



PRODUCT SUMMARY

V_{DSS}	I_D	$R_{DS(on)}$ (m-ohm) Max
100V	8	120 @ $V_{GS} = 10V$
	4	150 @ $V_{GS} = 4.5V$



ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous ^a @ $T_C = 25\text{ }^{\circ}\text{C}$ -Pulse ^b	I_D	11	A
	I_{DM}	25	A
Drain-Source Diode Forward Current ^a	I_S	4	A
Maximum Power Dissipation ^a	P_D	25	W
		10	
Operating Junction and Storage Temperature Range	T_J, T_{STG}	- 55 to 150	$^{\circ}\text{C}$

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient ^a	R_{thJA}	125	$^{\circ}\text{C/W}$
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Note

a. Surface Mounted on FR4 Board, $t \leq 10\text{sec}$.

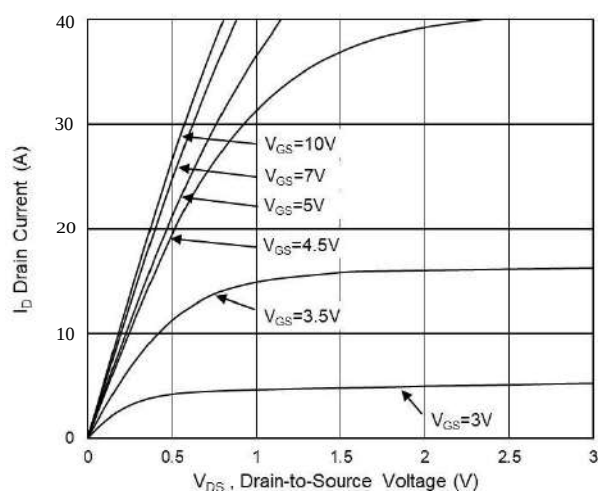
b. Pulse width limited by maximum junction temperature.

Parameter	Symbol	Condition	Min	Typ ^c	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V , I _D = 250uA	100			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 80V , V _{GS} = 0V			1	uA
Gate-Body Leakage	I _{GSS}	V _{GS} = ±20V , V _{DS} = 0V			±100	uA
ON CHARACTERISTICS ^b						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250uA	1.2	1.8	2.5	V
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10V , I _D = 8A		92	120	m-ohm
		V _{GS} = 4.5V , I _D = 4A		120	150	
Forward Transconductance	g _{fs}	V _{DS} = 10V , I _D =2A		11		S
DRAIN-SOURCE DIODE CHARACTERISTICS ^b						
Diode Forward Voltage	V _{SD}	V _{GS} = 0V , I _s = 4A			1.2	V
DYNAMIC CHARACTERISTICS ^c						
Input Capacitance	C _{ISS}	V _{DS} = 50V , V _{GS} = 0V f = 1.0MHz		185		pF
Output Capacitance	C _{OSS}			31		pF
Reverse Transfer Capacitance	C _{RSS}			2.8		pF
SWITCHING CHARACTERISTICS ^c						
Turn-On Delay Time	t _{D(ON)}	V _{DD} = 50V , I _D = 4A V _{GEN} = 10V R _L = 3 ohm R _{GEN} = 3ohm		4.8		ns
Rise Time	t _r			19		ns
Turn-Off Delay Time	t _{D(OFF)}			17		ns
Fall Time	t _f			6.2		ns
Total Gate Charge	Q _g	V _{DS} = 50V I _D = 8A V _{GS} = 10V		3.6		nC
Gate-Source Charge	Q _{gs}			0.68		nC
Gate-Drain Charge	Q _{gd}			0.9		nC

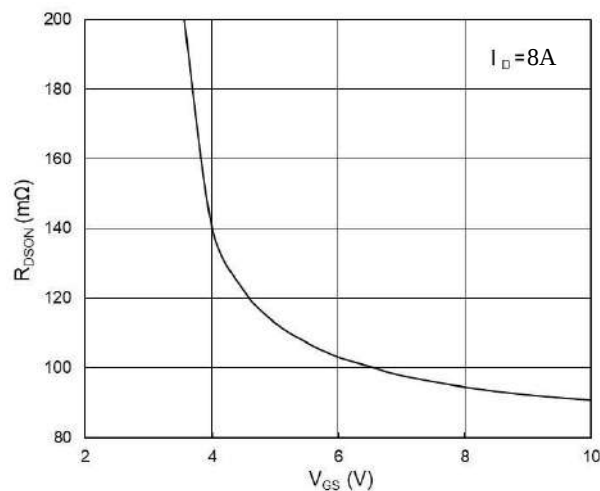
Note

b. Pulse Test Pulse width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.

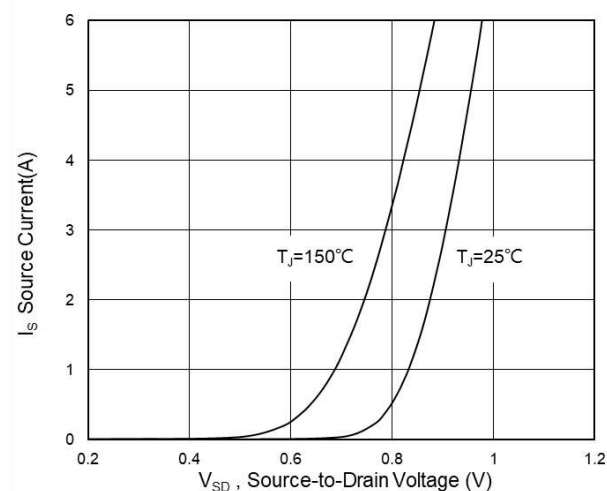
c. Guaranteed by design, not subject to production testing.



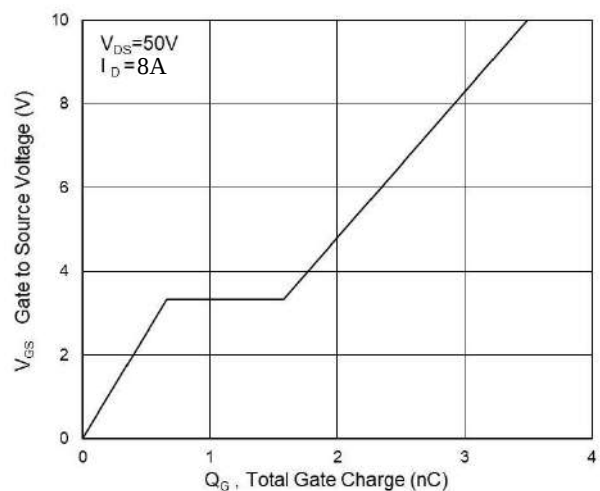
Typical Output Characteristics



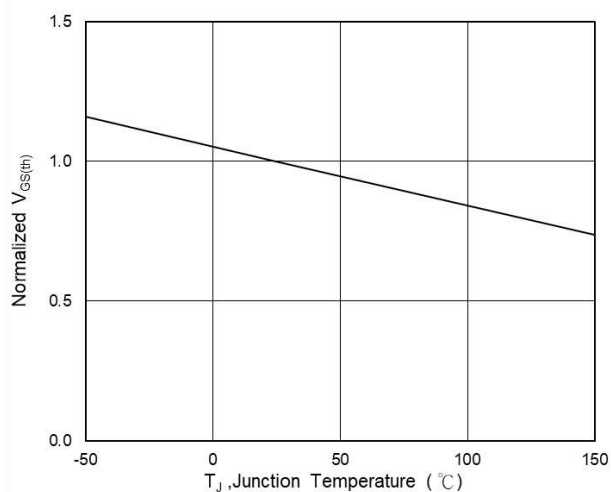
On-Resistance vs G-S Voltage



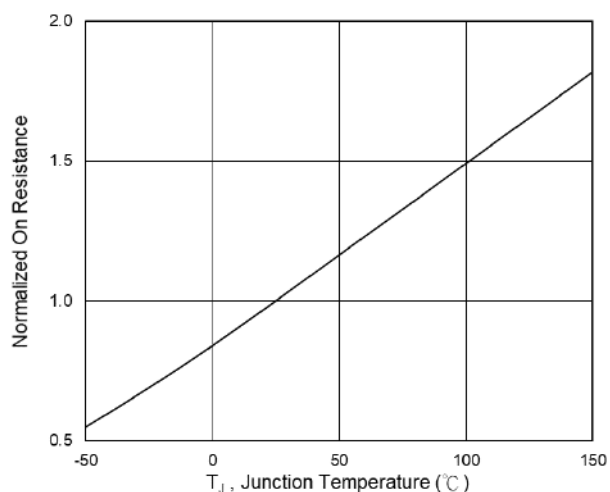
Source Drain Forward Characteristics



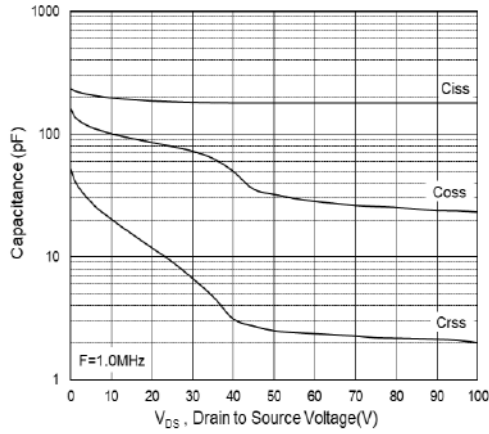
Gate-Charge Characteristics



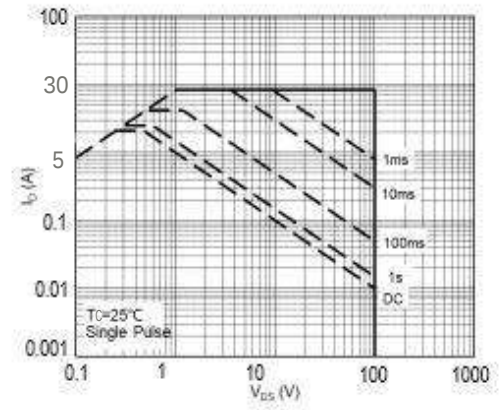
Normalized $V_{GS(th)}$ vs T_J



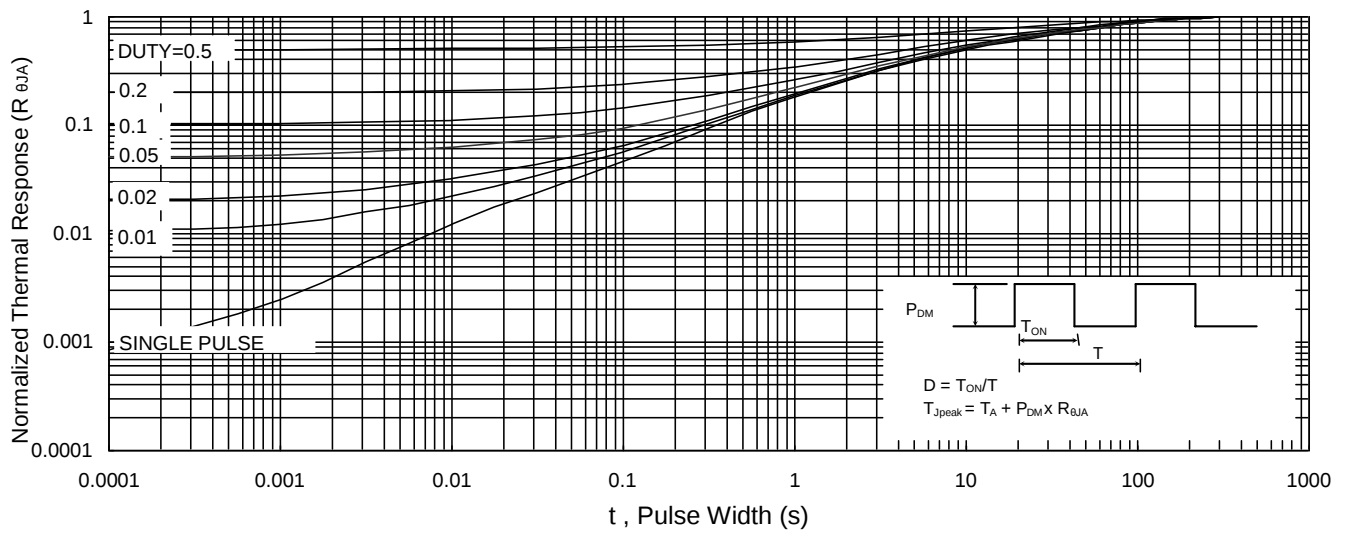
Normalized $R_{DS(on)}$ vs T_J



Capacitance



Safe Operating Area



Normalized Maximum Transient Thermal Impedance